Radiation induced Single Event Effects in the ATLAS MDT-ASD front-end chip

C. Posch, E. Hazen

Boston University, CAS Physics, 590 Commonwealth Ave, Boston, MA
cposch@ohm.bu.edu, hazen@bu.edu

Abstract

Single Event Effect (SEE) tests of the MDT-ASD, the ATLAS MDT front-end chip [9][10] have been performed at the Harvard Cyclotron Lab. The MDT-ASD is an 8-channel drift tube read-out ASIC fabricated in a commercial 0.5μm CMOS process (AMOS14TB). The chip contains a 53 bit register which holds the setup information and an associated shift register of the same length plus some additional control logic. 10 test devices were exposed to a 160 MeV proton beam with a fluence of $1.05 \cdot 10^{9}$ p·cm^{-2}·s^{-1} up to ≥$4.4 \cdot 10^{12}$ p·cm^{-2} per device. After a total fluence of $4.46 \cdot 10^{13}$ p ·cm^{-2}, 7 soft SEEs (non-permanent bit flips in the registers) and 0 hard/destructive SEE (e.g. latch-ups, SEL) had occurred. The simulated fluence for 10 years of LHC operation at nominal luminosity for worst case location MDT components is $2.67 \cdot 10^{11}$ h·cm^{-2}

The rate of SEUs in the ASD setup register for all of ATLAS, derived from these numbers, is 2.4 per day. It is foreseen to update the active registers of the on-detector electronics at regular intervals. Depending on the length of the update intervals, the SEU rate is very manageable and will not cause any significant degradation in performance of the ATLAS muon detector. The worst case impact of one SEU is the loss of eight channels out of 360.000 for the time of one update interval and occurs with a rate of ~ 1 per month.

1. Radiation environment

The MDT-ASD will reside and work in the Muon Spectrometer part of the ATLAS detector and thus will be exposed to the LHC radiation environment. The worst case location for the ATLAS MDT read-out electronics in terms of radiation levels is the inner end-cap (End-cap 1) close to the beam pipe. The expected fluence at this location for 10 years of ATLAS operation at nominal LHC luminosity (Simulated Radiation Level SRL_{see}) is $2.67 \cdot 10^{11}$ hadrons/cm^2. According to ATLAS RHA guidelines [2][3], this number has to be multiplied by several safety factors in order to calculate the total test exposure. The resulting fluence is $1.33 \cdot 10^{12}$ hadrons/cm^2.

2. ASIC fabrication process

The MDT-ASD is a full-custom mixed signal ASIC which has been designed for and fabricated in a commercial 0.5 μm N-well triple-metal CMOS process named AMOS14TB. The foundry is HP-Agilent. The process has a linear capacitor option consisting of polysilicon over an active N+ diffusion in an N-well (2250 aF/μm²). The process is silicided yielding very low polysilicon and diffusion resistivities. There is a "silicide" block layer available which allows exclusion of silicide over polysilicon but not over diffusion. This feature is used for polysilicon resistors. The nominal operating voltage for this process is 3.3 V.

The MDT-ASD is composed of full-custom analog blocks as well as library standard cells and pads. The design is based on MOSIS scalable CMOS (SCMOS) design rules [8]. These rules are generally more conservative than the process-specific vendor design rules. The minimum well-to-active spacing in MDT-ASD is 3 μm, which results in an increased latchup threshold (see Appendix). No further special radiation hardness improving layout techniques have been employed in the design.

3. Irradiation facility

The radiation test was done at the Harvard Cyclotron Laboratory at Harvard University, Cambridge, MA. The synchrocyclotron produces a max. 160 MeV proton beam with variable fluence of up to $3 \cdot 10^{10}$ protons/sec. The beam diameter can be adjusted from 0.1 cm to 30 cm. The calibration system uses a "Faraday cup" and a Keithley electrometer.

For this irradiation, the beam was set up to deliver 158 MeV proton at a fluence of $1.05 \cdot 10^{9}$ p·cm^{-2} ·s^{-1} with a beam diameter of 1.7 cm completely covering the die. The beam setup was verified by radiographs.

Each of 10 devices received a fluence of ≥ $4.4 \cdot 10^{12}$ p·cm^{-2} resulting in a total of $4.46 \cdot 10^{13}$ p·cm^{-2}. Details of the beam calibration can be inquired from [1].

4. Test setup and online monitoring

For Single Event Upset (SEU) monitoring the test system periodically reads all on-chip register contents, compares them to an initial state and re-writes the registers. Every bit flip is recorded and time stamped. The period of this read-write cycle is approximately 3 seconds. The power consumption of the DUT is monitored to catch Single Event Latchups (SEL).

During irradiation the DUT is biased and run under its nominal operating conditions, however there are no signals passed through the analog amplifier chain.

5. Results

The detailed results of the test are given in Table 1. The table contains for each tested component the number of SEEs observed (column 2), the position in the registers (columns 3, 4), the fluence at which the SEE occurred (column 4) and the total received fluence. The bits in the registers are simply numbered sequentially from 0 - 52 for the shift register and from 53 - 105 for the setup register. Only bit flips in the setup register affect the operation of the device. Note that three of four bit flips in the shift register provoke a flip in the corresponding setup register cell.

After a fluence of $4.46 \cdot 10^{13}$ p·cm^{-2}, a total of 7 soft SEEs (Single Event Upsets, SEUs) occurred. No hard/destructive SEEs (stuck bits, latch-ups) were observed[1].

Table 1. Results of the SEE test for each DUT. Columns 3 and 4 contain the register position, column 5 the fluence where the SEU occurred

Chip ID	# SEU	Shift Reg bit	Setup Reg bit	at p/cm^2	total p/cm^2
1	2	39	92	2.64E+012	4.40E+012
2	1	52	-	1.76E+011	4.61E+012
3	0	-	-	-	4.40E+012
4	0	-	-	-	4.76E+012
5	2	46	99	1.76E+012	4.41E+012
6	0	-	-	-	4.41E+012
7	0	-	-	-	4.41E+012
8	0	-	-	-	4.41E+012
9	2	29	82	3.53E+012	4.41E+012
10	0	-	-	-	4.41E+012
Total SEU	7			Total fluence	4.46E+013

The total fluence of $4.46 \cdot 10^{13}$ p·cm^{-2} divided by the number of occurred SEUs yields $6.38 \cdot 10^{12}$ p·cm^{-2} average fluence per SEU. With the simulated fluence for 10 years of LHC operation (including the simulation safety factor 5) SRL_{see} of $1.33 \cdot 10^{12}$ h·cm^{-2}, this results in a average number of 0.2 SEUs per device in 10 years. ATLAS MDT will contain 46'000 ASD devices, yielding a total of 9595 SEUs in 10 years or 4.8 SEUs per day, assuming 200 calendar days per year of operation. As only bit flips in the setup register affect the functionality of the devices, this number can be divided by a factor of 2. This leads to a final result of 2.4 SEUs per day for all MDT-ASDs in ATLAS.

It is foreseen to update the active registers of the on-detector electronics at regular intervals. Depending on the length of the update intervals, this SEU rate is very manageable and will not cause any significant degradation in performance of the MDT detector. The worst case impact of one SEU is the loss of eight channels out of 360'000 for the time of one update interval. The length of the update interval has not been determined yet, however preliminary estimates claim that updates could happen every few minutes.

Depending on the position of the bit flip in the setup register, the impact on the device ranges from no effect to inaccurate/wrong data to a temporary shut-off of one channel [10]. A bit flip in the most-significant-bit of the Threshold DAC could set the threshold for all 8 channels to a value that caused the chip to produce useless data (worst case). All other parts of the setup register are less delicate and would only cause minor effects like changing setup parameters of the charge ADC. The chips main function, drift time measurement, would not be affected significantly. Thus the probability of the worst case impact is 1 out of 53 SEUs.

[1] See appendix for data of Single Event Latch-up (SEL) tests on the AMOS14TB process.

6. Conclusion

Proton irradiation of 10 devices up to a total fluence of $4.46 \cdot 10^{13}$ p·cm^{-2} yielded enough statistics to make a solid prediction on average fluence per SEE per device for the MDT-ASD. The relevant numbers are 0.2 SEUs per device in 10 years and 2.4 SEUs per day for all of ATLAS. No hard/destructive SEE (e.g. latch-ups) occurred.

The SEU rate is very manageable and will not cause any considerable degradation in performance of the ATLAS MDT detector. The worst case impact of one SEU is the loss of eight channels out of 360'000 for the time of one update interval and happens with a probability of 1 out of 53 SEUs or approximately once per month. Table 2 contains a summary of the relevant numbers.

Table 2. SEE results summary

$4.46 \cdot 10^{13}$ p·cm^{-2}	Total test fluence
$6.38 \cdot 10^{12}$ p·cm^{-2}	Average fluence per SEU (7)
$1.33 \cdot 10^{12}$ h·cm^{-2}	Fluence for 10 years ATLAS (SRL_{see})
0.2086	Average SEU per device (10 years)
46'000	Number of devices
9'595	Total SEU - all devices (10 years)
959.5	SEU / year
4.80	SEU / day (assuming 200 days running)
2.40	SEU / day (only setup register)
~ 1	Worst case SEU / month

With the fluence reached in this test and the good statistics, we believe to obtain a high level of confidence on the prediction of the SEE behavior of the device. As the fabrication process is well established and runs since 1996 with closely monitored, very stable process parameters [6], we are convinced that this test also qualifies the MDT-ASD volume production lot in terms of SEE hardness.

7. Appendix

Aerospace Corp. Single Event Latchup (SEL) tests on commercial CMOS processes [7]

Single event latchup testing was performed with both a single shot laser system and with accelerated heavy ions ranging in effective LET from 5.6 MeV/mg/cm2 to greater than 120 MeV/mg/cm2. Figure 1 indicates that the HP 0.5μm devices range in latchup threshold from 63 LET for a 1.5 μm well-to-active spacing to greater 100 LET for a 4.5 μm well-to-active spacing device. HP 0.5μm latchup thresholds improve at the rate of ~12 LET per micron of increased well-to-active spacing. Bias of the HP devices was 3.3 V during both ion and laser testing [7].

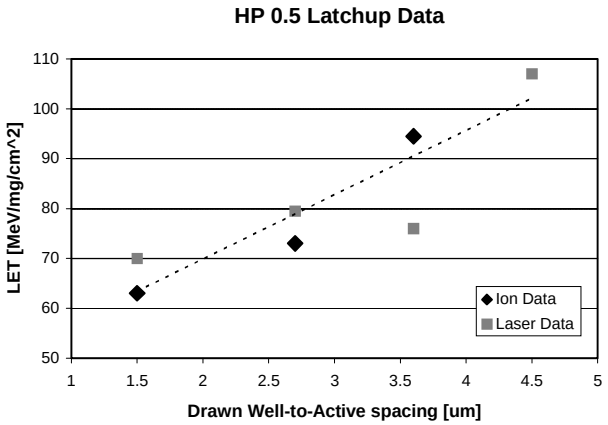

Figure 1. Latchup threshold in LET versus distance between biased N-well and grounded Active regions

The MDT-ASD is designed using SCMOS scalable design rules, which are generally more conservative than the process-specific vendor design rules. The minimum well-to-active spacing in MDT-ASDs is 3 μm, resulting in a 81 LET latchup threshold.

A recent simulation study has shown that the maximum energy deposition occurring with non-negligible probability in the LHC radiation environment will correspond locally to a LET lower than 50 $MeV \cdot cm^2 \cdot mg^{-1}$. This will happen only in the very rare case of a nuclear interaction in tungsten, which is used in certain ICs for connection purposes between metal layers [4][5].

8. References

[1] E. Cascio, Harvard Cyclotron Laboratory, 44 Oxford St., Cambridge, MA.

[2] M. Dentan, Overview of the ATLAS Policy on Radiation Tolerant Electronics, Proceedings of the 6th Workshop on Electronics for LHC Experiments, CERN-2001-005/CERN-LHCC-2001-034, Oct. 2001.

[3] M. Dentan et. al., ATLAS Radiation Hard Electronics Web Page, http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm

[4] F. Faccio, C. Detcheverry, M. Huhtinen, First evaluation of the Single Event Upset (SEU) risk for electronics in the CMS experiment, CERN CMS NOTE 1998/054 (1998)

[5] P. Jarron, G. Anelli, T. Calin, J. Cosculluela, M. Campbell, M. Delmastro, F. Faccio, A. Giraldo, E. Heijne, K. Kloukinas, M. Letheren, M. Nicolaidis, P. Moreira, A. Paccagnella, A. Marchioro, W. Snoeys, R. Velazco, Deep submicron CMOS technologies for the LHC experiments, Nuclear Physics B (Proc. Suppl.) 78 (1999) 625 - 634

[6] MOSIS Integrated Circuit Fabrication Service, web site, MOSIS Parametric Test Results for HP AMOS14TB Runs, http://www.mosis.org/Technical/Testdata/hp-amos14tb-prm.html

[7] J.V. Osborn, D.C. Mayer, R.C. Lacoe, S.C. Moss, and S.D. La Lumondiere, Single event latchup characteristics of three commercial CMOS processes, in Proceedings of 7th NASA Symposium on VLSI design, 1998

[8] J. Pi, MOSIS Scalable CMOS design rules (Rev. 7), the MOSIS Service, Information Sciences Institute, University of Southern California, Aug. 1995.

[9] C. Posch, S. Ahlen, E. Hazen, J. Oliver, CMOS front-end for the MDT sub-detector in the ATLAS Muon Spectrometer - development and performance, Proceedings of the 7th Workshop on Electronics for LHC Experiments, CERN-2001-005/CERN-LHCC-2001-034, Oct. 2001.

[10] C. Posch, E. Hazen, J. Oliver, MDT-ASD, CMOS front-end for ATLAS MDT, ATLAS Muon Note, ATL-MUON-2002-003, CERN, June 2001.