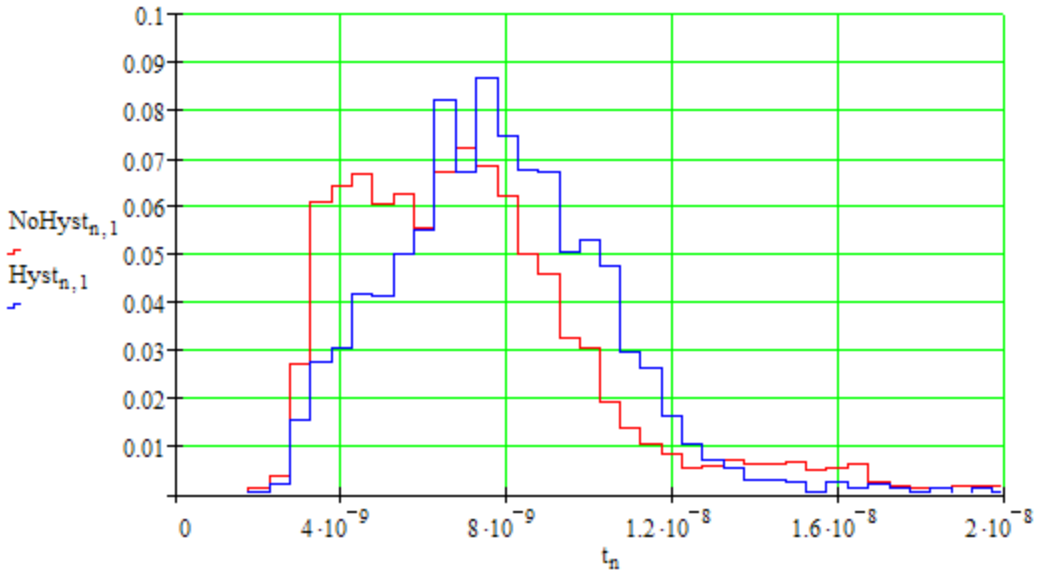
Note on MDT-ASD LVDS output pulses due to thermal noise hits

The following measurements were taken with a mezz card plugged into the mezz test stand which provides dummy terminations (390Ω). This resulted in a steady stream of noise hits as usual, which were then recorded on a digital scope. In TOT (time-over-threshold) mode we expect these pulses to be rather narrow. Six or eight nanoseconds would be typical with some of the widths extending down to 1ns-2ns. In ADC mode, we expect the minimum width to be set by the Wilkinson gate width setting.

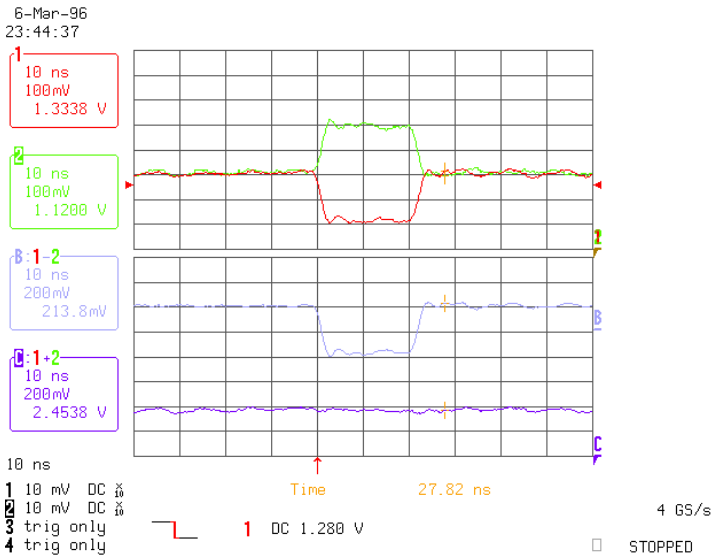
A pulsewidth distribution of the LVDS output signal in TOT mode is shown below. The red trace shows the case with hysteresis setting of 0 counts while the blue trace has a small hysteresis setting of 3 counts[1].



This distribution is about as expected. Adding a few counts of hysteresis has the effect of increasing the peak of the distribution and reducing the number of very narrow pulses. The actual pulse shape of the LVDS signal is also as expected.

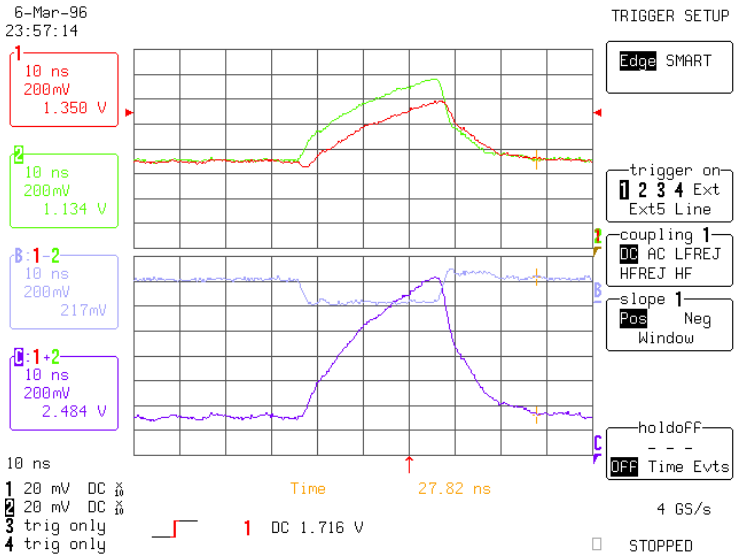
[1] Hysteresis setting is quoted in counts as opposed to mv to avoid confusion as to the scale conversion. Actual value has been measured to be 1.5mv/count.

In ADC mode, the situation is a bit messier. The bulk of the noise hits produce fairly normal looking output pulses as shown below. [2]



The top two traces are the output LVDS levels, the third trace is the difference of the two, and the bottom trace is the sum, or 2x the common mode level. A proper LVDS signal from the ASD should have a differential swing of 400mv and a common mode swing of zero. Note that the pulse width is ~20ns and is controlled by the setting of the Wilkinson gate width. With zero hysteresis setting, about 85% of the noise pulses look like the traces above.

However, a smaller proportion of the pulses take the following form.

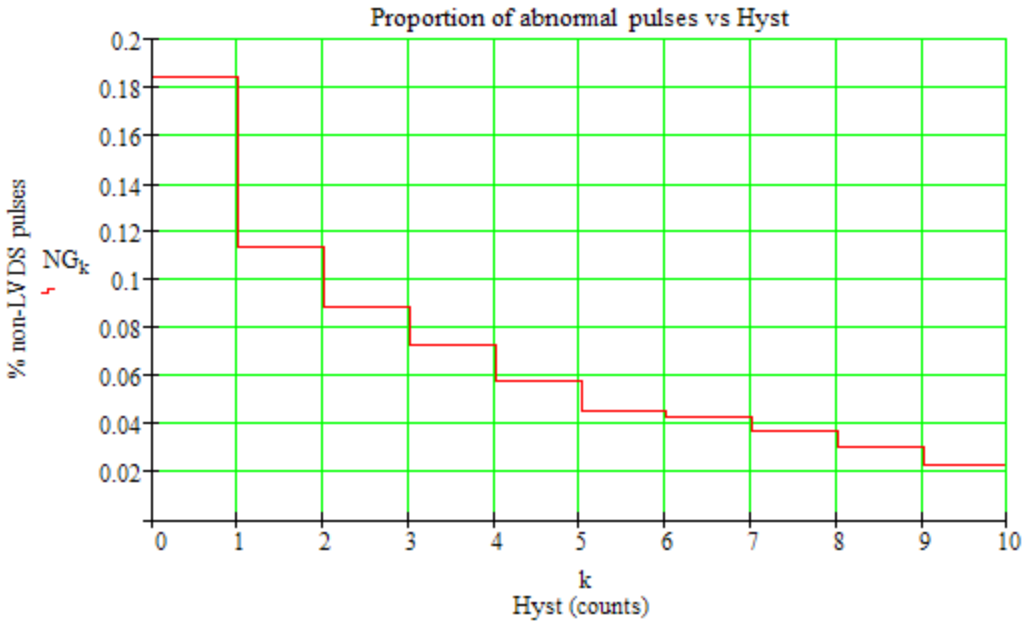


Note that in the above case, the differential signal is only half its expected size and there is a common mode swing of about 0.5 volts. The root of this phenomenon certainly

[2] Sorry for the faded looking tiff files.

resides in the Wilkinson gate generator circuits and likely represents a meta-stable condition of the flip-flops of this circuit. Its likely that very small noise pulses fail to fully flip the flip-flops which then fail to produce clean rail to rail output pulses. The effect has not yet been studied in SPICE simulations.

The effect of hysteresis setting on these abnormal output pulses was studied. The result is that increasing hysteresis setting reduces the proportion of abnormal pulses as shown in the following plot.



As shown in the above plot, adding hysteresis does not eliminate the abnormal pulses, but it does reduce their frequency from 18% with no hysteresis down to about 2% with 10 counts or 15mv. Note that hysteresis produces symmetrical threshold shifts which must be subtracted from the threshold setting. So, for example, if we wish to use five counts of hysteresis, the threshold must be reduced by 5x1.5mv = ~8mv.