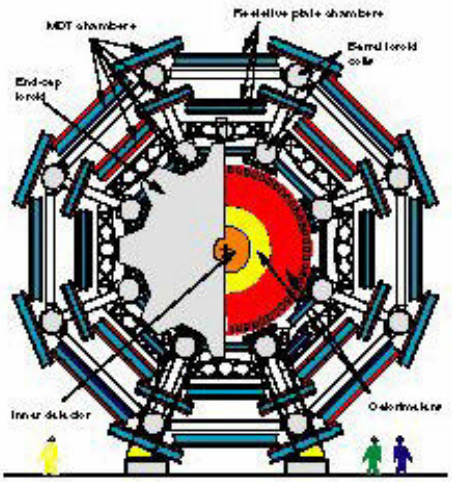

ATLAS

Muon Spectrometer

MDT-ASD

Parameter Setup Manual

Ver 1.03

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Table of Contents

Version	Date	Comment
1.02	29 Apr 03	Original
1.03	6 Jun 03	Fixed Rundown current & Disc2 threshold setup params

0 General

The MDT-ASD has 11 programmable registers which total 53 bits as shown in the table below (Channel Mode is considered two 8-bit registers)

JTAG bit	Description	LSB/code
[0:7]	Channel mask register [0:7]	bit 0 channel 0
[8:10]	Calibration injection capacitor select [2:0]	bit 10 LSB
[11:18]	Main threshold DAC (DISC1) [7:0]	bit 18 LSB
[19:21]	Wilkinson ADC threshold DAC (DISC2) [2:0]	bit 21 LSB
[22:25]	Hysteresis DAC (DISC1) [3:0]	bit 25 LSB
[26:29]	Wilkinson ADC integration gate [3:0]	bit 29 LSB
[30:32]	Wilkinson ADC rundown current [2:0]	bit 32 LSB
[33:35]	Deadtime [2:0]	bit 35 LSB
[36:37]	Channel mode – channel 0 (top) [1:0]	‘0x’ Active ‘10’ Force Lo ‘11’ Force Hi
[38:39]	Channel mode – channel 1 [1:0]	
[40:41]	Channel mode – channel 2 [1:0]	
[42:43]	Channel mode – channel 3 [1:0]	
[44:45]	Channel mode – channel 4 [1:0]	
[46:47]	Channel mode – channel 5 [1:0]	
[48:49]	Channel mode – channel 6 [1:0]	
[50:51]	Channel mode – channel 7 (bottom) [1:0]	
[52]	Chip mode	‘0’ ADC, ‘1’ ToT

In order to accurately program the chip, one needs to know the relationship between the downloaded register values and the corresponding parameters, such as Wilkinson gate width, rundown current, etc. These relationships are extracted for each chip during production chip test and are recorded into a database. They are described in the following sections and typical values derived from measurements of approximately 10k chips. The data base of tested chips is found at http://hepldb.harvard.edu/elec1/ASDmain.asp

A complete description of the MDT-ASD, including all programmable parameters, can be found at
http://doc.cern.ch//archive/electronic/cern/others/atlnot/Note/muon/muon-2002-003.pdf

A description of the chip testing procedure, database parameters, and quality codes, can be found in the Chip Tester User’s Manual at
http://huhepl.harvard.edu/~oliver/UsersManual.pdf

1 Discriminator

1.1 Threshold

Recommended threshold setting is determined by the chip's gain, noise levels, and offset voltages. The gain or "sensitivity" of the ASD depends on whether or not the inputs are "terminated", meaning whether or not the card is plugged into a terminated chamber (or dummy terminations). When terminated, the gain is reduced by approximately 20%. Threshold dispersion refers to the rms spread in offset voltages as measured over a large number of channels. Typical values for a terminated MDT-ASD are;

Parameter	Typical value	Comments
Sensitivity	8.9 mv/fc	Delta response
Single electron response (SPICE)	1.65 mv/pe	@ 2*10^4 gas gain
RMS noise	7.8 mv	
enc	5500 electrons rms	Delta function referred
enc	4.7 pe	Primary electron referred
Nominal operating threshold	- 40mv	
Equivalent threshold in pe	23.7 pe	
Threshold dispersion	3.9 mv	See ChipTesterDatabase

Note that the amplifier's response to a single electron in the MDT is computed by convoluting the assumed shape of the pulse tail with the delta response. This is done in SPICE and the results quoted above. In order to operate the chip at 5σ above thermal noise level, the nominal threshold must be set to;

$$V_{thr(nominal)} = -40 \text{ mv}$$

In terms of primary electrons, this is equivalent to

$$PE(thr) = \frac{40mv}{1.65\, mv/pe} = 23.7\ primary\ \ electrons$$

This value is higher than the target value of 20 primary electrons so that to achieve the target value, the MDTs would have to operate at a slightly higher gas gain of 2.4*10^4.

1.2 Noise rates

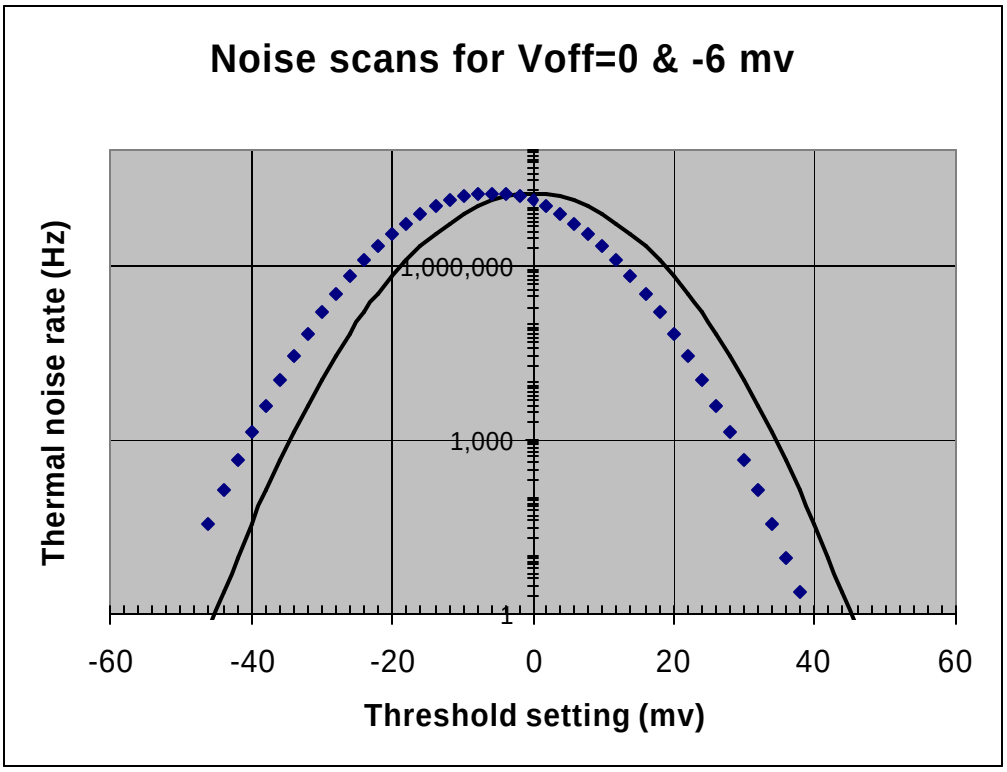
For any particular threshold setting, we expect to get random noise hits which are Poisson distributed in time and a Gaussian function of threshold as shown below.

$$R(x) = R_0 \cdot e^{-\frac{(x-V_{off})^2}{2 \cdot s^2}}$$

where R_0 is the maximum rate of hits, V_{off} is the measured offset voltage of the channel, s is the rms noise voltage, and x is the threshold setting. The parameters R_0 , V_{off} , and σ are extracted during production chip testing for each channel and placed in the production database. Typical values for peak rates are ~20MHz so that for zero offset, we expect thermal noise rates of

$$R(5\cdot s) \approx (20MHz)\cdot e^{-\frac{5^2}{2}} \approx 75Hz$$

Typical noise plots are shown below for offsets of 0 and – 6 mv respectively.



Note that the offset of – 6 mv results in a noise rate of about 50 fold and we therefore expect this channel to be a "hot channel". In general, for a channel with non-zero offset, when operating at 5σ, we expect the noise hit rate to increase by the factor;

$$R'/R = e^{\frac{-5\cdot V_{off}}{s}} \approx 2x \ factor\ per\ mv\ of\ negative\ offset$$

When taking such noise scans, neither the AMT-3, nor the DAQ systems can measure noise rates beyond about one half megahertz or so. The chip test procedure, however, uses a counter to measure the rates directly, and has confirmed the Gaussian nature of this curve over the entire threshold range.

For each chip, the database contains a signed offset correction which is taken as the mean between the maximum and minimum offsets of the eight channels on the chip. This correction should be added to the nominal desired threshold setting. "Quality 1" chips are selected by cutting on maximum offset spread of less than a 12 mv total across all eight

channels of the chip. Thus, if the offset correction is downloaded, no channel will have an effective offset of worse than 6 mv in either direction.

Of course, none of this precludes operation at more conservative threshold values of -44 mv, for example, or even higher. The final recommended nominal threshold setting will have to come from on-chamber noise and resolution studies.

1.3 Hysteresis

Hysteresis is utilized simply to provide clean transitions of the discriminator through its firing point.

Hysteresis is set by a 4-bit code as follows;

$$Hysteresis \cong 1.25mv \cdot N$$

where $N = 0,1,...15$

Hysteresis does, by necessity, cause an effective threshold shift, which is equal to the nominal hysteresis setting. Thus a hysteresis setting of 2.5 mv, for example, shifts the actual firing point by 2.5 mv away from zero. In this example, a setting of -40 mv, will result in an effective threshold of -42.5 mv. Thus, to maintain an actual threshold of -40 mv, the threshold register must be set to -38 mv. The final recommendation for hysteresis setting must be gained from experience, but a reasonable starting point would be in the range of 1.25 mv to 5.0 mv.

2 Wilkinson parameters

2.1 Gate width

Wilkinson gate width refers to the charge integration period at the leading edge of the pulse. It is set by a 4-bit code, N, which corresponds to the physical gate width as follows,

$$Tgate = (11 + 1.5 \cdot N)ns$$

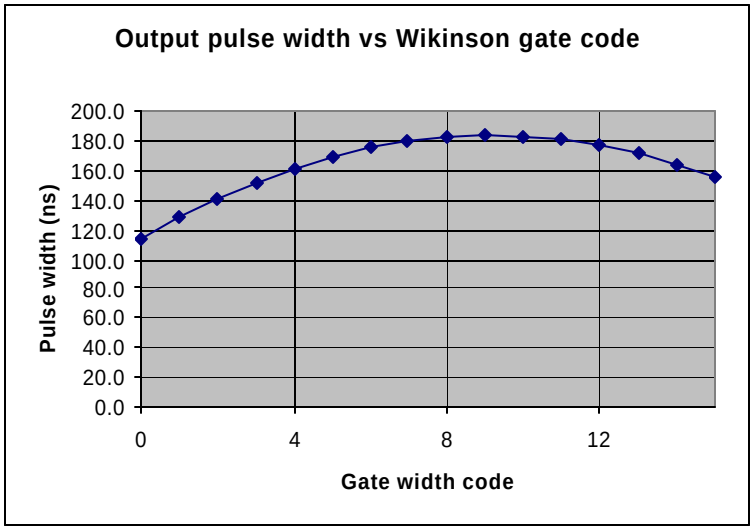
While the gate width is not directly observable, its effect on the output pulse width is measured and characterized by a quadratic expression, whose parameters are found in the chip-test database.

$$T_{out} = A\_gate \cdot N^2 + B\_gate \cdot N + C\_gate$$

Typical values are shown below.

Parameter	Typical value	Units
A_gate	-0.83	ns
B_gate	15.2	ns
C_gate	114	ns
Typical T_{out} at N = 0	114	ns
Typical T_{out} at N=15	155	ns

A typical measurement of output pulse width vs W_{gate} programming code is shown below.



Note that this curve corresponds to measurements made during production chip testing using delta function charge injection. Measurements made on-chamber will be different.

2.2 Rundown current

Rundown current[see note [1]] refers to the programmable discharge current of the hold capacitors after the Wilkinson integration period. It can be set to a nominal value of between 2.4 μa and 7.3 μa in steps of 0.7 μa. The current cannot be measured directly however, but its effect on the output pulsewidth is recorded and its parameterized coefficients are placed in the database.

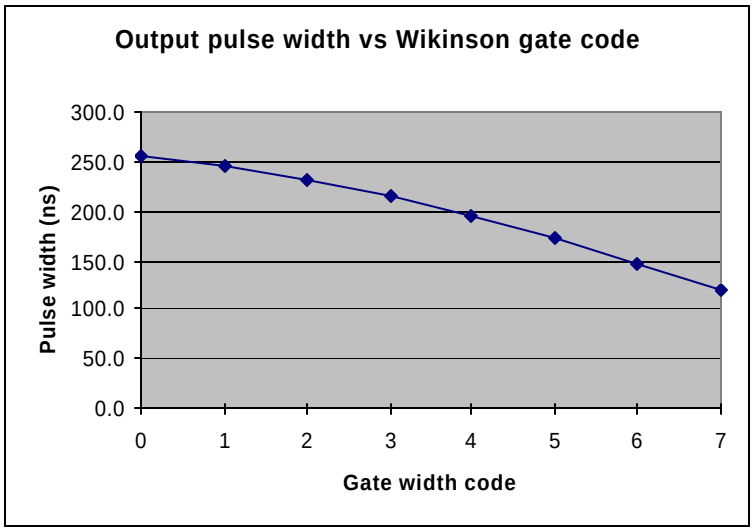
$$T_{out} = A\_Rund \cdot Nbar^2 + B\_Rund \cdot Nbar + C\_Rund$$

Note [1] : 6 June 2003 – Rundown current actually decreases with increasing register value, while rundown time increases. Thus, the formulas have been modified to be a function of Nbar which is the bit for bit inverse of N. Thus, the register is to be loaded with N, while time is computed as a function Nbar.

where N takes values of 0,1, ... 7 . Typical values are shown below.

Parameter	Typical value	Units
A_Rund	-0.83	ns
B_Rund	15.2	ns
C_Rund	114	ns
Typical value at Nbar=0	256	ns
Typical value at Nbar=7	120	ns

A plot of typical pulse width values corresponding to programming code is shown below.



2.3 Disc2 threshold

This refers to the discriminator whose firing defines the end of the rundown period. Its effect on the output pulse width is exceedingly minimal. While the Chip Tester can determine its characteristics, this feature has not been implemented and no database entries are made.

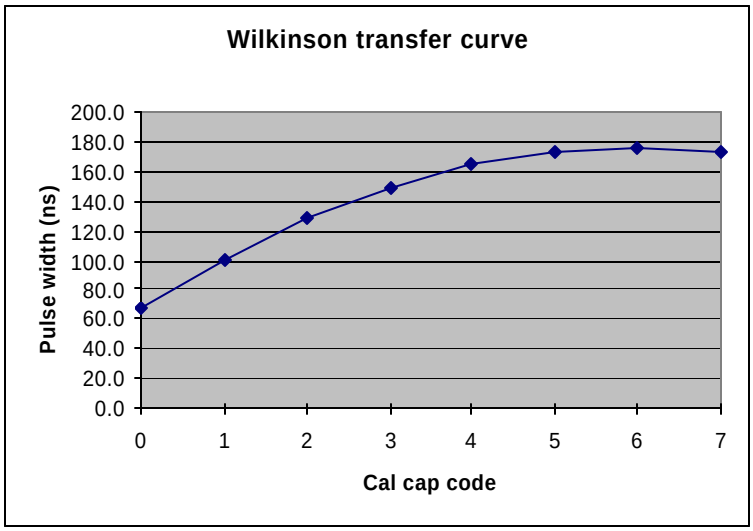
2.4 Transfer curve

The Wilkinson transfer curve measures the output pulse width as a function of input charge for each channel of the chip. Since input charge is injected by the on-chip calibration capacitors its value depends on the size of the applied strobe step and the number of caps. This applied step size has been set in the Chip Tester but its important to note that its value on the Mezzanine cards may be somewhat different.

There are eight cal_inject capacitors per channel, each of which has a nominal value of 50 ff. Once a channel is enabled by setting its mask bit, anywhere from 1,2, ... 8 caps can be selected.

It should be noted that a “channel 0” effect has been discover in the chip tester which invalidates the parameters extracted for this channel. The technical reasons for this have nothing to do with the chip, but are an artifact of the tester. It is due to the close proximity of a STROBE line to the ASD’s channel 0 input line and there is nothing to be done about it at this point. Values are placed in the database, but note that channel zero data are not particularly meaningful and should be excluded when taking averages or histograms. This feature has been observed in the transfer curve test, but not in any of the others.

Parameter	Typical value	Units
A_Xfer	-3.1	ns
B_Xfer	36.8	ns
C_Xfer	67.1	ns
Typical value at N=0 [2]	67	ns
Typical value at N=7	173	ns



Note that codes = 0,1, ... , 7 correspond to 1,2, ... , 8 calibration caps.

2.5 Deadtime

Programmable deadtime is measured by a double pulse / binary search routine during chip testing and its parameters placed in the database. It is defined as the time between the trailing edge of one pulse and the leading edge of the second; in other words, the time minimum time between pulses. The allowed separation between leading edge of one pulse and leading edge of the second, is therefore the sum of the average deadtime plus the average pulse width. Its max value will be in the neighborhood of 600 ns. It should be noted that the design target for deadtime was 1,000ns and earlier versions of Mini-DAQ

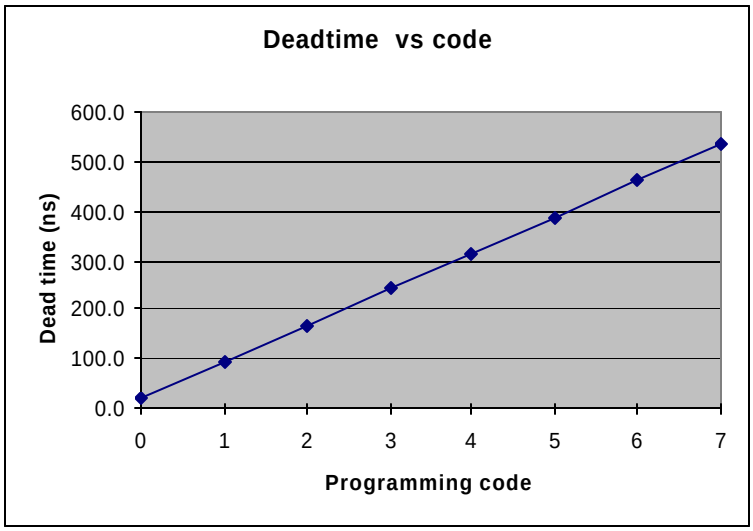
[2] N = programming code

refers to this maximum. Deviations of the manufactured chips from the design models resulted in this smaller figure.

Deadtime is a linear function of programming code. Typical values and plots are shown below.

Parameter	Typical value	Units
A_Prog	74	ns
B_Prog	18.3	ns
Typical value at N=0	74	ns
Typical value at N=7	535	ns

A typical plot is shown below.



3 Summary : Nominal operating settings

Below is a table of nominal settings used in the Chip Tester and database. We expect those values to be very close to the ones used on the mezz cards on-chamber.

Parameter	No. bits	Nominal value	Nominal code[3]		Expression
Disc1 threshold	8	-40 mv	N	108	(N - 128)*2 mv
Disc1 hysteresis	4	2.5 mv	N	2	N*1.25 mv
Wgate	4	20 ns	N	6	(11 + 1.5*N) ns
Disc2 threshold	3	30 mv	Nbar	1	(14 + 16*Nbar) mv
W_Rundown	3	5.9 µa	Nbar	5	(2.4+0.7*Nbar) µa
Deadtime	3	535 ns	N	7	(74 + 18.3*N)

[3] Note that for W_rundown and Disc2_threshold, the expression and recommended operating point are given in terms of Nbar, the bit-for-bit complement of N. The reason for this is, well, trust me there's a good reason.