MDT–ASD Production Chip Tester

– Specification –

DRAFT

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1. TESTS

Tests will be done by analog / digital circuitry under the control of an FPGA. Each test will be initiated by means of a Command Register and results will be reported by a Status register and buffer memory. Some tests will be simply pass/fail while others will result in a data block in the buffer. At the conclusion of each test, the data buffer is read into the computer for analysis and display. The buffer memory be implemented as a FIFO. In the following "Result" blocks, the FIFO output is taken from the top.

1.1. Digital I/O

Read-Write

This test is for verifying integrity of serial shift and shadow registers. It is not intended to functionally test any other features of the chip.

Send test bit stream to shift register and then load into shadow register. Flush shift register with zeros, then shift shadow register down and out. Compare results. Repeat with several test strings.

Hardware requirements: -

Result: Pass/Fail flag in Status register

Test #	CR bit	description	Word count
1.1	0	Digital I/O functionality	1

1.2. DC Tests

1. Bias circuit

Using external DAC, sweep current from –500 μA to +500 μA into Vb2 node. Current is injected by a voltage DAC into a resistor connected to Vb2. Therefore voltage at resistor input must also be monitored by ADC. Monitor voltages Vb1… Vb4. Use these data to plot standard bias voltage characteristics. Extract NFET and PFET transistor parameters (K, Vth).

Hardware requirements: 8-bit DAC, voltage output, plus resistor at Vb2 node. 4 × 12-bit ADC channels at nodes Vb1 - Vb4.

Result: Five words for each of the 256 possible DAC settings for total block size of 1280 words.

Test #	CR bit	description	Word count
1.2.1	1	Bias circuit DC levels	1280

Memory map:

Vres_0*
Vb1
Vb2
Vb3
Vb4
Vres_1*
Vb1
Vb2
*
*
Vres_255*
Vb1
Vb2
Vb3
Vb4

* DAC codes or measure? Would need additional ADC channel.

2. *Preamp input levels*

Check common mode and differential input voltage levels. Voltages are monitored by ADC through resistor.

Hardware requirements: 16 × 12-bit ADC channels plus (large) resistor at pre-amp inputs.

Result: Sixteen words in data buffer as follows.

Test #	CR bit	description	Word count
1.2.0	2	* DAC codes or measure? Would need additional ADC channel. Preamp input levels	16

Memory map:

Vina0
Vinb0
Vina1
Vinb1
Vina2
Vinb2
Vina3
*
Vina7
Vinb7

3. *LVDS levels*

Use chip and channel mode control bits to force output LVDS levels Hi and Lo. Monitor common mode and differential LVDS levels. This also monitors two of the four output modes (Force HI, Force LO). Levels will be forced in two patterns; Even channels Hi, odd channels lo and then vice versa.

Hardware requirements: 16 × 12-bit ADC channels at LVDS outputs.

Result: Thirty two words in memory. The first 16 correspond to Even channels Hi. The second 16 correspond to Odd channels Hi.

Test #	CR bit	description	Word count
1.2.3	3	LVDS levels	16

Memory map:

Vouta0
Voutb0
Vouta1
Voutb1
Vouta2
Voutb2
Vouta3
*
*

4. *Power consumption*

Measure supply current at nominal VDD. Measure supply current vs. variable VDD?

Hardware requirements: 1 ADC channel

Result: 1 word

Test #	CR bit	description	Word count
1.2.4	4	Power consumption	1

1.3. Dynamic Tests

There will be two sources of calibration pulses used for dynamic tests. The primary source will be the internal cal_inject capacitors. The capacitor bank will give use three bits of dynamic range while a DAC setting will allow fine control of amplitude. A secondary source of cal_inject pulses will be through known external capacitors to the pre-amp inputs. This will allow an absolute calibration of the internal cal_inject caps.

Hardware requirements: 2 × 8-bit DAC at STR/STRB, 8 (16) × 8-bit DAC at external capacitors.

1. Analog monitor

Oscilloscope output and trigger will be provided to monitor Ch7 analog output. This may be used for diagnostics or to provide a visual on-line pulse display for signal quality (amplitude and peaking time). Additionally, we may implement a Sample/Hold circuit and ADC to capture peak values of analog output for standard linearity tests.

Baseline plan is to use discriminator threshold scan to reconstruct analog pulse. This is done in Time over Threshold (TOT) mode. For a fixed cal_inject pulse height, record leading and trailing edge time relative to pulse injection. This is done for each of the 128 DAC settings and for each channel of the ASD. When threshold is above pulse, no time stamp will occur. In this case, data = 00 will be returned.

Result: One leading edge time and one trailing edge time for each DAC settings; 256 words for each of 8 channels. 2048 (2k) words total.

Test #	CR bit	description	Word count
1.3.1	5	Analog monitor	2048

Memory map:

VTH0_ch0_lead
VTH0_ch0_trail
VTH0_ch1_lead
VTH0_ch1_trail
VTH0_ch2_lead
*
VTH1_ch0_lead
VTH1_ch0_trail
VTH1_ch1_lead
VTH1_ch1_trail
*
*
VTH255_ch7_lead
VTH255_ch7_trail

2. *Cal_inject cross calibration*

Same technique as 1.3.1 but use external injection capacitors. The capacitors will be grouped in an EVEN bank and an ODD bank so that they are not all hit simultaneously. The data are the same format as 1.3.1

Result: One leading edge time and one trailing edge time for each DAC settings; 256 words for each of 8 channels. 2048 (2k) words total.

Test #	CR bit	description	Word count
1.3.2	6	Cal_inject cross calibration	2048

Memory map:

VTH0_ch0_lead
VTH0_ch0_trail
VTH0_ch2_lead
VTH0_ch2_trail
VTH0_ch4_lead
*
VTH0_ch1_lead
VTH0_ch1_trail
VTH0_ch3_lead
VTH0_ch3_trail
*
VTH1_ch0_lead
VTH1_ch0_trail
VTH1_ch2_lead
*
VTH255_ch7_lead
VTH255_ch7_trail

3. *Disc1 threshold*

Set threshold DAC and sweep input pulse height to find firing point. This will be done in a binary search routine. This is done for each Disc 1 threshold setting starting from a minimum value above noise floor.

Result: Memory block containing charge injection pulse height DAC value found by binary searcher. The threshold DAC will be scanned over the top 96 of 128 values. Thus memory block will be 96 words.

Test #	CR bit	description	Word count
1.3.3	7	Disc1 threshold	96

Memory map:

VTH32_pulseDAC
VTH33_ pulseDAC
VTH34_ pulseDAC
*
VTH127_ pulseDAC

4. Disc1 hysteresis

Varying the Disc1 hysteresis current has an effect on the Disc1 firing and un-firing points. For a single fixed input signal and Disc 1 threshold value (set to e.g. 50% of DA_3 peak), the hysteresis DAC is swept through each of its 8 values and leading and trailing edge of ToT are recorded.

Result: One leading edge time and one trailing edge time for each of 8 hysteresis DAC setting for 1 of 8 channels, 16 words total.

Test #	CR bit	description	Word count
1.3.4	8	Disc1 hysteresis	16

Memory map:

HYST0_lead
HYST0_trail
HYST1_lead
HYST1_trail
*
HYST7_lead
HYST7_trail

5. Wilkinson gate

In Wilkinson Mode, varying the Wilkinson Gate DAC varies the LVDS output pulse width. In Time-over-Threshold Mode, pulse width is narrow and constant. This test is used to verify the Wilkinson and TOT Mode states as well as the Wilkinson gate width. For a fixed set of parameters (injection signal, VTH1, VTH2, rundown current), leading and trailing edge of output pulse are recorded on 1 of 8 channels for all of 16 gate DAC settings.

Result: Leading edge and trailing edge TDC times for 1 of 8 channels and each of 16 gate DAC settings, 32 words total.

Test #	CR bit	description	Word count
1.3.5	9	Wilkinson gate	32

Memory map:

GATE0 _lead
GATE0 _trail
GATE1 _lead
GATE1 _trail
*
GATE15 _lead
GATE15 _trail

6. Wilkinson rundown

In Wilkinson Mode, vary the rundown DAC current and observe changes in the output pulse width. For a fixed set of parameters (injection signal, VTH1, VTH2, Integration gate), leading and trailing edge of output pulse are recorded on all of 8 channels for all of 8 Rundown Current DAC settings

Result: Leading edge and trailing edge TDC times for 1 of 8 channels and each of 8 Rundown Current DAC settings, 16 words total.

Test #	CR bit	description	Word count
1.3.6	10	Wilkinson rundown	16

Memory map:

RDC0_lead
RDC0 _trail
RDC1 _lead
RDC1 _trail
*
RDC7 _lead
RDC7 _trail

7. Disc2 threshold

In Wilkinson Mode, vary the Disc2 threshold setting and observe the effect on output pulse width. For a fixed set of parameters (injection signal, VTH1, rundown current, Integration Gate), leading and trailing edge of output pulse are recorded on all of 8 channels for all of 16 VTH2 DAC settings

Result: Leading edge and trailing edge TDC times for 1 of 8 channels and each of 8 VTH2 DAC settings, 16 words total.

Test #	CR bit	description	Word count
1.3.7	11	Disc2 threshold	16

Memory map:

VTH2.0 _lead
VTH2.0 _trail
VTH2.1 _lead
VTH2.1 _trail
*
VTH2.7 _trail
VTH2.7 _trail

8. Wilkinson transfer characteristic

In Wilkinson Mode, vary the input signal threshold setting and observe the effect on output pulse width. For a fixed set of parameters (VTH1, VTH2, Integration Gate, Rundown Current), leading and trailing edge of output pulse are recorded on all of 8 channels for e.g. 32 injection pulse DAC settings.

Result: Leading edge and trailing edge TDC times for each of 8 channels and 32 input pulse settings, 512 words total.

Test #	CR bit	description	Word count
1.3.8	12	Wilkinson transfer characteristic	512

Memory map:

INJP0_ch0_lead
INJP0_ch0_trail
INJP0_ch1_lead
*
INJP0_ch7_trail
INJP1_ch0_lead
INJP1_ch0_trail
*
*
INJP32_ch7_trail

9. Deadtime

In Wilkinson Mode, set the output deadtime to each of 8 values. Inject pulse pairs into the cal_inject circuits and sweep the pulse separation. Observe the reappearance of the second pulse in the LVDS output. Record 2 TDC values (leading edge of each pulse of the pulse pair) corresponding to the true deadtime for each of 8 channels and each of 8 deadtime DAC settings

Result: Leading edge pair TDC times for each of 8 channels and each of 8 deadtime DAC settings, 128 words total.

Test #	CR bit	description	Word count
1.3.9	13	Deadtime	128

Memory map:

DEAD0_ch0_pulse1
DEAD0_ch0_pulse2
DEAD0_ch1_pulse1
*
DEAD0_ch7_pulse2
DEAD1_ch0_pulse1
DEAD1_ch0_pulse2
*
*
DEAD7_ch7_pulse2

2. HARDWARE CONFIGURATION

2.1. System architecture

The basic scheme is a 3-piece arrangement consisting of a commercial PCI digital I/O card, the main controller board with the controller FPGA and all other active components (ADCs, DACs, S/H etc.) plus a daughter board with the chip socket and passive circuitry (power supply filters etc.). The PCI I/O card will be connected to the main board by a ribbon cable, the daughter board sits directly on the main board (board-to-board connector) or is connected via a short ribbon cable. The purpose for this second separation is to be able to change the chip socket independently as it is a wearing part.

2.2. The main controller and DAQ board

2.3. Controller special tasks

1. Time to Digital conversion

Time to Digital Conversion is required for measurement of output pulse leading and trailing edges with a bin size requirement of the order of 1 ns. Xilinx DLL based TDCs have been implemented and can provide bin size in this range, depending on clock speed. This option is attractive as a Xilinx Virtex II FPGA will already be present on the main card.

2. Averaging

All multiple test invoking and averaging is triggered and conducted by the FPGA.

3. Binary search

Test 1.3.3 requires a binary search engine to be implemented in the FPGA.

3. IMPLEMENTATION

3.1. Hardware requirements

1. Analog

- 1 × 8-bit DAC, voltage output, plus resistor at Vb2 node.
- 2 × 8-bit DAC, voltage output, at STR/STRB.
- 8 (16) × 8-bit DAC at external injection capacitors.
- 10 (18) × fast analog switch.
- 4 × 12-bit ADC channels at nodes Vb1 - Vb4.
- 16 × 12-bit ADC channels plus resistors at pre-amp inputs.
- 16 × 12-bit ADC channels at LVDS outputs.
- 1 × 12-bit ADC channel for VDD current.
- Voltage regulator, supply filter for ASD

2. Interface Analog - Controller

3. Controller

- Virtex II FPGA (?)

4. Interface Controller - PCI digital I/O card

5. PCI digital I/O card

3.2. Command register

Test #	CR bit	Description	Word count
1.1.1	0	Digital I/O functionality	1
1.2.1	1	Bias circuit DC levels	1280
1.2.2	2	Preamp input levels	16
1.2.3	3	LVDS levels	16
1.2.4	4	Power consumption	1
1.3.1	5	Analog monitor	2048
1.3.2	6	Cal_inject cross calibration	2048
1.3.3	7	Disc1 threshold	96
1.3.4	8	Disc1 hysteresis	16
1.3.5	9	Wilkinson gate	32
1.3.6	10	Wilkinson rundown	16
1.3.7	11	Disc2 threshold	16
1.3.8	12	Wilkinson transfer characteristic	512
1.3.9	13	Deadtime	128
		Total words	**6226**

3.3. Status register