MDT-ASD: Amplifier Simulations and Measurements

The MDT-ASD analog channel consists of the following basic blocks (Figure 1): Pre-amplifier, shaper (filter), discriminator (threshold comparator), Wilkinson charge ADC and output stage. This note concentrates on simulation and measurement results of all amplifier stages, namely the pre-amplifier, the differential amplifiers DA1 through DA4 and the analog output pad drivers (not shown in the block diagram).

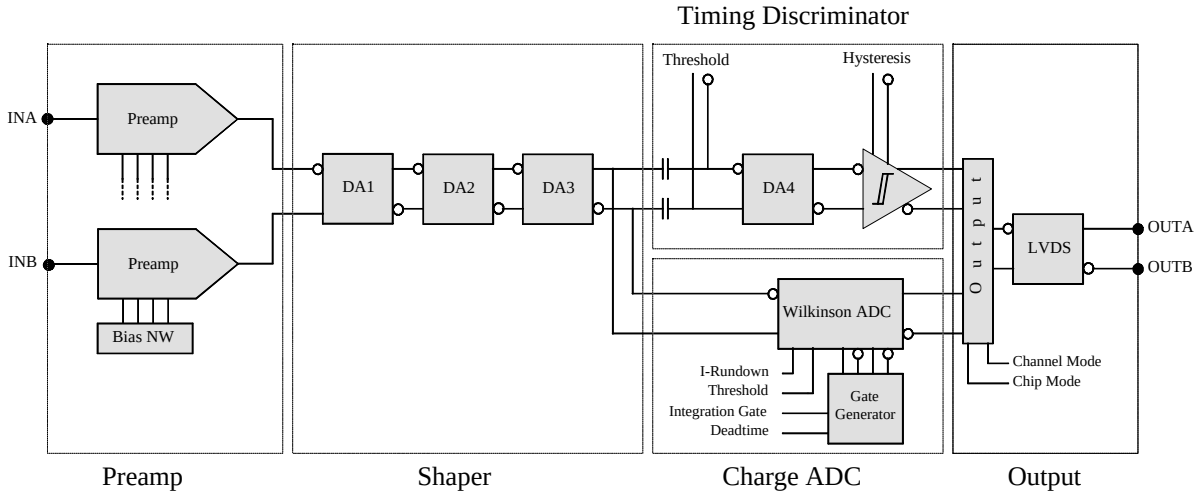

Figure 1. **MDT-ASD channel: Block diagram**

1. Pre-Amplifier

Figure 2 shows the simulated signal transfer characteristic of the MDT pre-amplifier. The input signal is a voltage step function with a rise time of 2 ns applied to an ideal capacitor of 100 fF at the pre-amplifier input. The range is 50 – 800 mV yielding the charge range of 10 – 160 fC. The small signal frequency response of the pre-amplifier is shown in Figure 3. The input signal is a 1 mV AC signal.

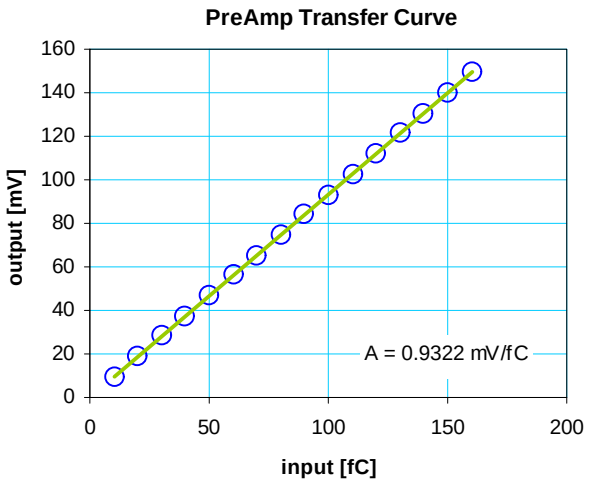

Figure 2. **MDT-ASD pre-amplifier: SPICE simulation of the transfer characteristic (output peak voltage vs. input charge) shows good linearity over an extended input charge range (Nominal range ~ 10 – 80 fC). The amplification is 0.93 mV/fC [2].**

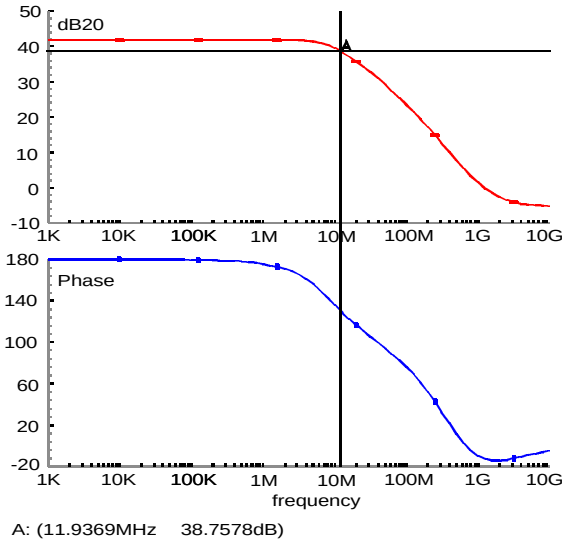

Figure 3. **MDT-ASD pre-amplifier frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of 41.75dB with the -3dB point at 11.49 MHz. The rolloff slope is -6dB/octave. The phase plot shows an initial phase shift of 180 degrees, decreasing to zero at ~ 700 MHz.**

2. Differential Amplifier Stages DA1 – DA4

Four differential amplifier stages DA1 through DA4 serve both as gain and as shaping amplifiers. The basic topology for all four amplifiers is identical while the feedback networks differ according to the desired frequency characteristics.

- DA1 is a simple gain stage with purely resistive feedback. The bandwidth is limited by the product of the feedback resistor and the load capacitance, typically consisting of the gate capacitances of the subsequent stages and the source/drain capacitances of the input and output transistor pairs. The gain is 4.5dB with a 3dB bandwidth of 45 MHz (Figure 5). The pulse peak voltage gain is in the order of 1.1 exhibiting sufficient linear behavior (Figure 4). DA1s main purpose is to ensure the signal being completely complementary.

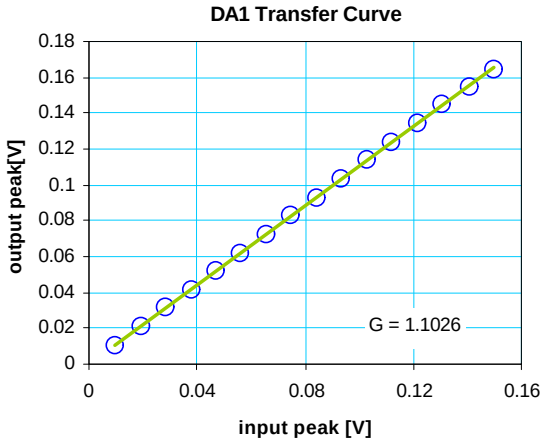

Figure 4. **Differential amplifier DA1: Output versus input pulse peak voltage. The linear region extends the working signal range by at least a factor of two.**

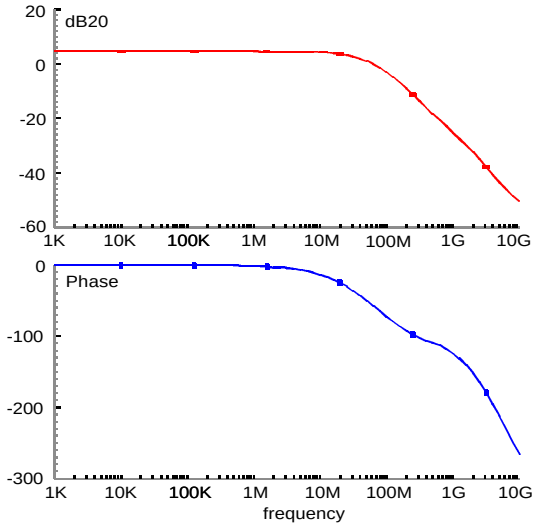

Figure 5. **Differential amplifier DA1 frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of 4.5dB with the -3dB point at 45 MHz. The rolloff slope is -6dB/octave. The phase plot shows an initial phase shift of 0 degrees, decreasing to -180 at ~ 3 GHz.**

- DA2 and DA3 constitute the shaping portion of the MDT-ASD. The desired combined shaping function has a bipolar characteristic. This frequency response is achieved by adding a series R-C branch in parallel to the resistive feedback in case of DA2 and by replacing the feedback resistor with a series R-C branch in DA3.

DA2 shows a linear peak voltage gain of 3.4 over the extended signal range (Figure 6) while DA3 exhibits a compressive transfer characteristic with a small signal voltage gain of ~ 3.2 (Figure 7). Again, the working signal range is roughly the first half of the plotted range.

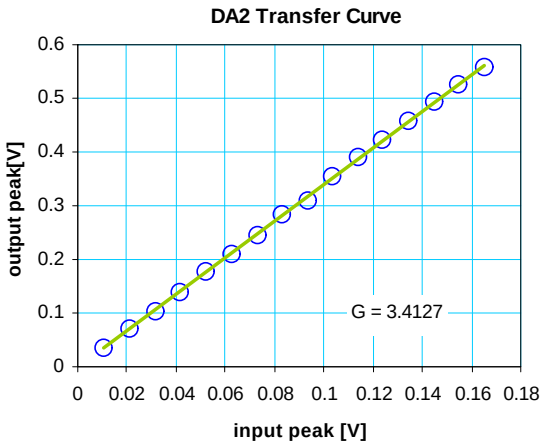

Figure 6. **DA2 output peak voltage vs. input peak voltage**

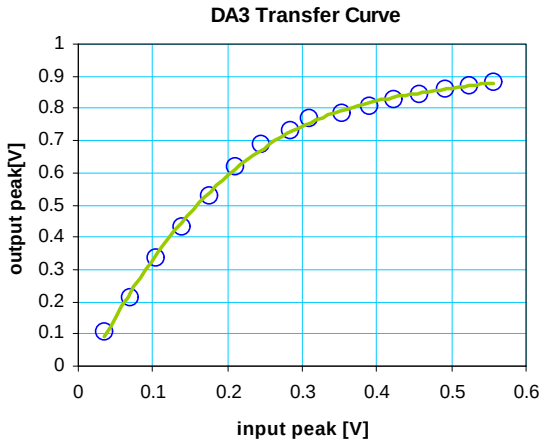

Figure 7. **DA2 output peak voltage vs. input peak voltage**

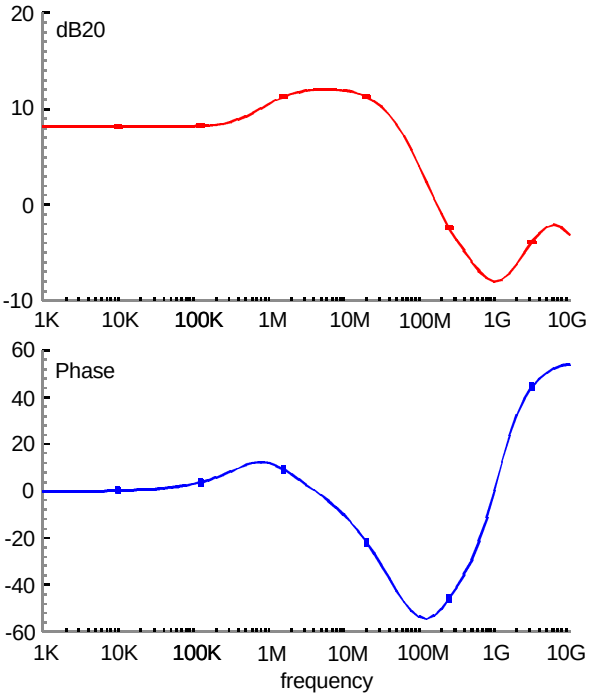

Figure 8. **DA2 AC characteristics**

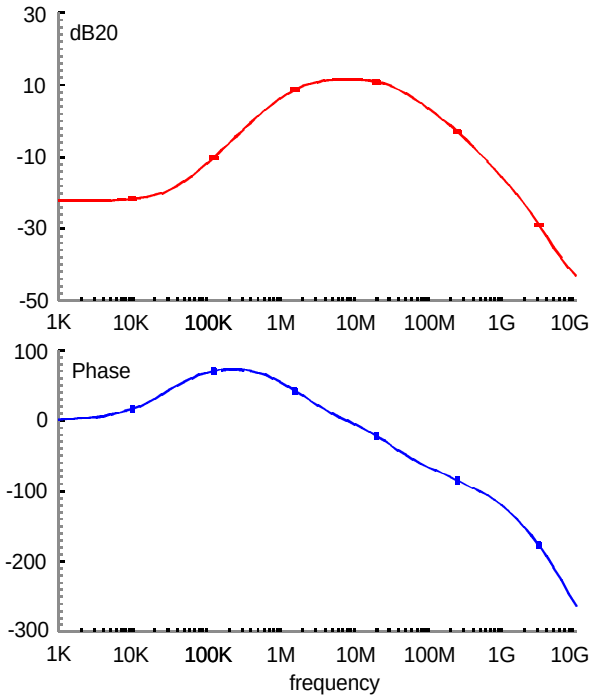

Figure 9. **DA3 AC characteristics**

The AC characteristics of the shaping amplifiers are shown in Figure 8 and Figure 9. The gain peak for both amplifiers is approximately 12dB in the range of 5 to 10 MHz.

- DA4 is the pre-comparator gain stage of the timing discriminator with a voltage gain of 5 to 6. The transfer curve, again covering twice the expected signal range, shows DA4 going to saturation very fast.

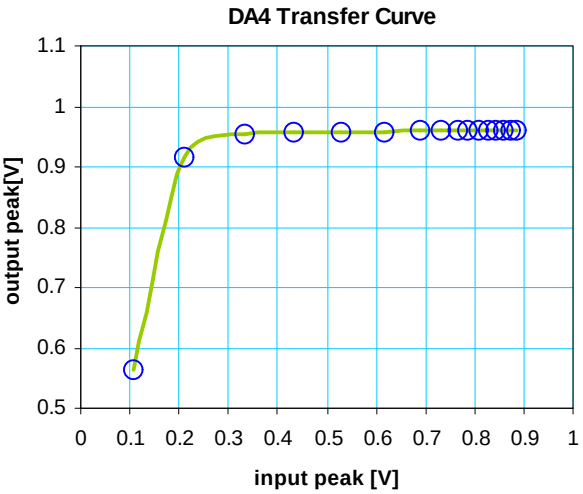

Figure 10. **Differential amplifier DA4: Output versus input pulse peak voltage (double dynamic range).**

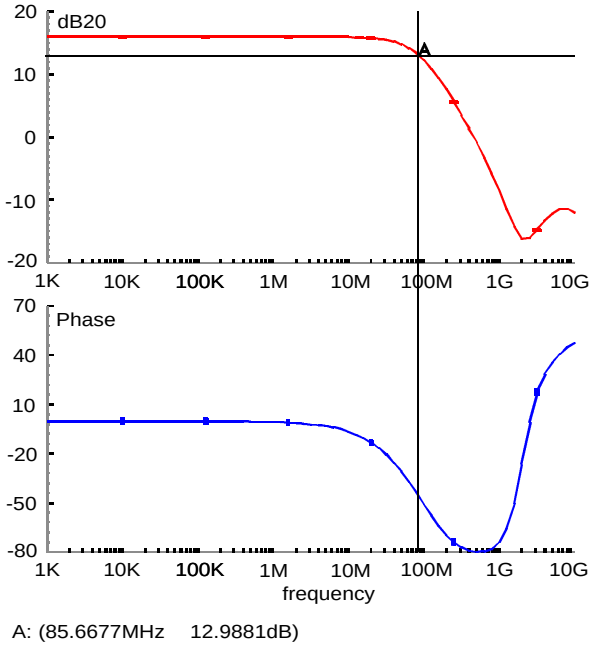

Figure 11. **Differential amplifier DA4 frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of 16dB with the -3dB point at 86MHz. The rolloff slope is -6dB/octave. The phase plot shows an initial phase shift of 0 degrees decreasing to -80 degrees at 400 MHz.**

3. Pre-Amplifier – Shaper: Combined Transfer Characteristic

The analog signal chain ends at DA3 output where the signal is tapped to be sent to the analog pad drivers and where the discriminator threshold is applied before the signal is put onto the pre-comparator amplifier DA4. The combined characteristics of the pre-amplifier – shaper chain are summarized in Figure 12 and Figure 13.

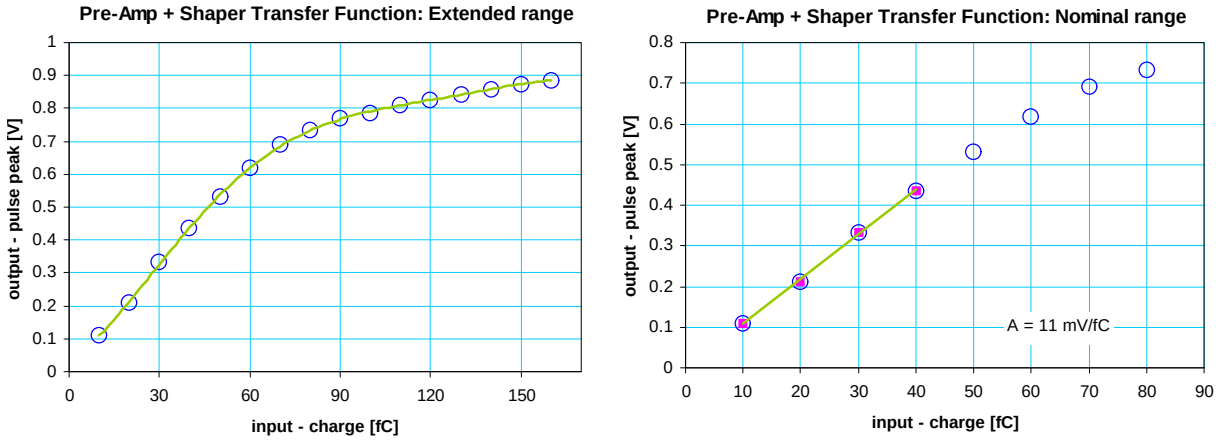

Figure 12. **Analog signal chain transfer characteristics: Extended (left) and nominal range (right). The linearity within the nominal range is adequate. The sensitivity of the pre-amp – shaper combination is 11 mV/fC.**

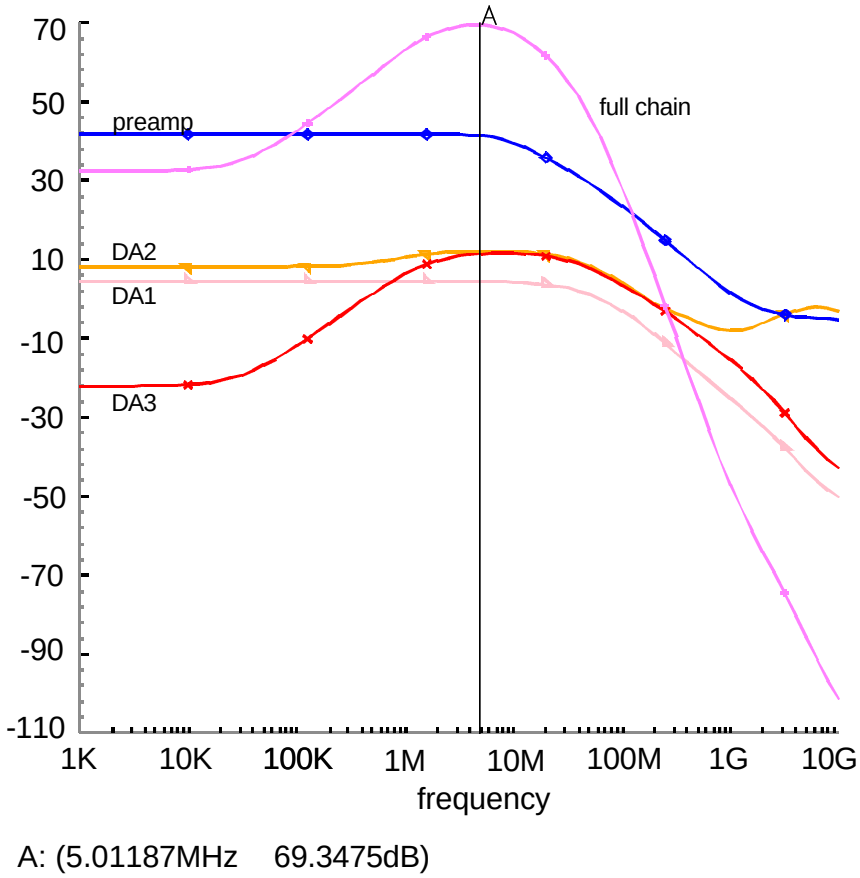

Figure 13. **Pre-amplifier – DA3 analog signal chain: AC frequency response; the amplifier chain exhibits a pass-band characteristic with a center frequency of 5 MHz. The high-pass part, mainly imposed by DA3, shows a corner frequency of 30 kHz and a slope of +6dB/octave (representing a first order high-pass filter). The low-pass section is a superposition of all four amplifier low-pass characteristics that have similar corner frequencies between 38 MHz and 44 MHz. The curve shows a -24dB/octave slope (or fourth-order low-pass filter behavior) above ~ 45 MHz. At approx. 500 MHz where DA2 goes flat again, the slope reduces to -18dB/octave (third order).**

The peak lies at 5 MHz showing a gain of close to 70dB.

4. Analog Chain: Time Domain Pulse Response

Figure 14 shows the measured and simulated pulse response of the analog signal chain pre-amplifier – DA3 including the analog output pad drivers (see section 5). The input signals in both cases are voltage steps (200, 550, 900, 1350 mV) with a rise time of 2 ns applied to a 50 fF capacitor at the pre-amplifier input.

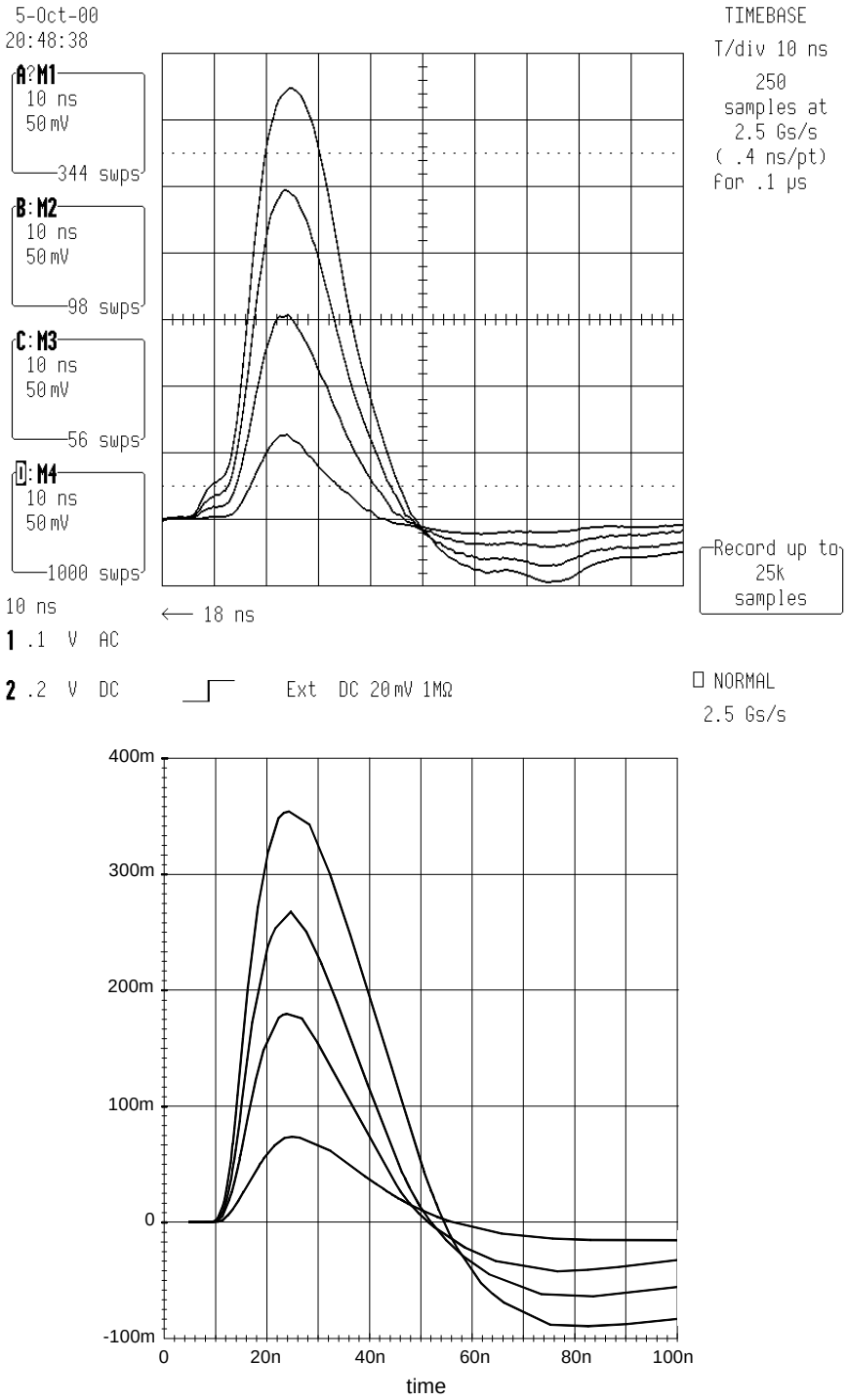

Figure 14. **Measured (top) and simulated pulse response of the analog signal chain. The input pulses are created by applying voltage steps to one on-chip test-pulse injection capacitor (50 fF). The rise time of the steps is 2 ns, the amplitudes are 200, 550, 900 and 1350 mV, yielding input charges of 10, 27.5, 45 and 67.5 fC.**

5. Analog Pad Driver

The pad driver has a voltage gain of –3.7dB and a bandwidth of 185 MHz (Figure 15).

Figure 16 shows the voltage of the analog output pulse peak measured at the analog output pad as a function of the input charge. The discrepancy between simulation and measurement is small which indicates that the used simulators and device models are reasonably accurate. The differences can also be caused by numerous other effects, including variations of process parameters. Measurement results assuming the on-chip calibration capacitors being 10% below designed value are added for illustration (solid blue line).

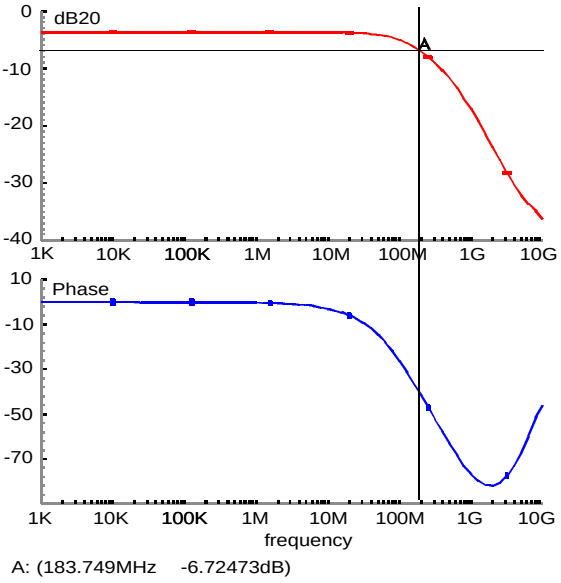

Figure 15. **Analog pad driver frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of -3.7dB with the -3dB point at 184 MHz. The rolloff slope is -6dB/octave.**

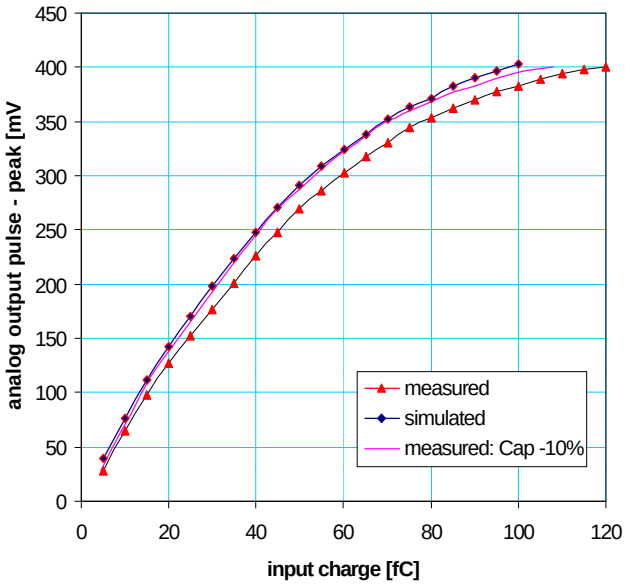

Figure 16 **Simulated and measured analog output pulse peak versus input charge using the calibration injection system. The blue solid line represents measurement results assuming the on-chip calibration capacitors being 10% lower than their designed value.**

All simulations were done using BSIM3 Version 3.1 Level 49 MOS transistor-models[1] and the AVANT® HSPICE simulator.

[1] The used NMOS and PMOS models can be found in the appendix.

Appendix

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.LIB v31

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+K3B     = -0.6826036    W0      = 5.954482E-6    NLX     = 1.160795E-8
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+U0      = 494.1066594   UA      = 5.793483E-10   UB      = 1.282667E-18
+UC      = 3.434774E-11  VSAT    = 1.259976E5     A0      = 0.9390877
+AGS     = 0.1848153     B0      = 2.222029E-6    B1      = 5E-6
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+DWB     = 1.235807E-8   VOFF    = -0.0896698     NFACTOR = 1.2143784
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+CDSCB   = 2.979369E-5   ETA0    = 1.712692E-3    ETAB    = 3.4153E-3
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+PDIBLC2 = 3.027171E-3   PDIBLCB = -0.1           DROUT   = 0.4026747
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+LW      = 0             LWN     = 1              LWL     = 0
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+CGSO    = 2.51E-10      CGBO    = 1E-11          CJ      = 5.06534E-4
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+K3B     = -1.4496401    W0      = 5.256776E-6    NLX     = 8.640935E-8
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+LKETA   = -2.10717E-3   PAGS    = 0.12532
*
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References

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