MDT-ASD: Serial data I/O and programmable parameters

It was found advantageous to be able to control or tune certain analog and functional parameters of the MDT-ASD, both at power-up/reset and during run time. Rather than applying external currents or voltages, it was chosen to send the control signals as digital data to the chip, where they are converted into physical quantities by custom Digital-to-Analog Converters (DACs) as required. A serial I/O data interface was implemented in the ASD, containing digital I/O ports, shift registers plus shadow registers and the required control logic. The data as well as the control signals and the shift register clock are generated by an FPGA[1] on the mezzanine card and are transmitted to the ASDs using a JTAG like protocol.

ASD serial data interface

The chosen ASD serial data interface architecture employs separate shift and working registers. The shift register is connected directly to digital input and output pads respectively. Its length is designed to hold a complete set of control bits (53). The data can be uploaded any time (asynchronously) to the shadow registers, which control the DACs, multiplexers etc. The architecture allows downloading the whole set of active bits from the shadow to the shift register in order to send them back to the controller for diagnostic or monitoring purposes. This can be done any time and does not interfere with the normal operation of the ASD.

The interface, for each data bit, consists of the shift register-cell, implemented as a static master-slave D flip-flop, the shadow register cell, realized as a static transparent latch and 2 two-in-one multiplexers (Figure 1).

The protocol requires 2 data lines (TO and FROM chip), 3 control lines (LOAD, HOLD, DOWN) and one clock line. The configuration allows extensive control over the data flow. HOLD mode keeps the data in the shift register by feeding back each cell with its own content. SHIFT mode shifts data right at the rising edge of the clock. LOAD active copies the bits in the shift register to the shadow register at any time (asynchronous). DOWN active copies the contents of the shadow registers to the shift register at the next rising clock edge (overrides SHIFT – HOLD). The ASD serial input expects the data to be stable at the rising edge of the clock ± a few nanoseconds. The controller will change data bits at the falling clock-edge. Thus data are stable at the input for the entire clock period with the sensitive rising edge in the middle. Data bits at the ASD serial data output also change state at the falling edge of the clock. ASDs thus can be daisy-chained to form a closed JTAG type control loop.

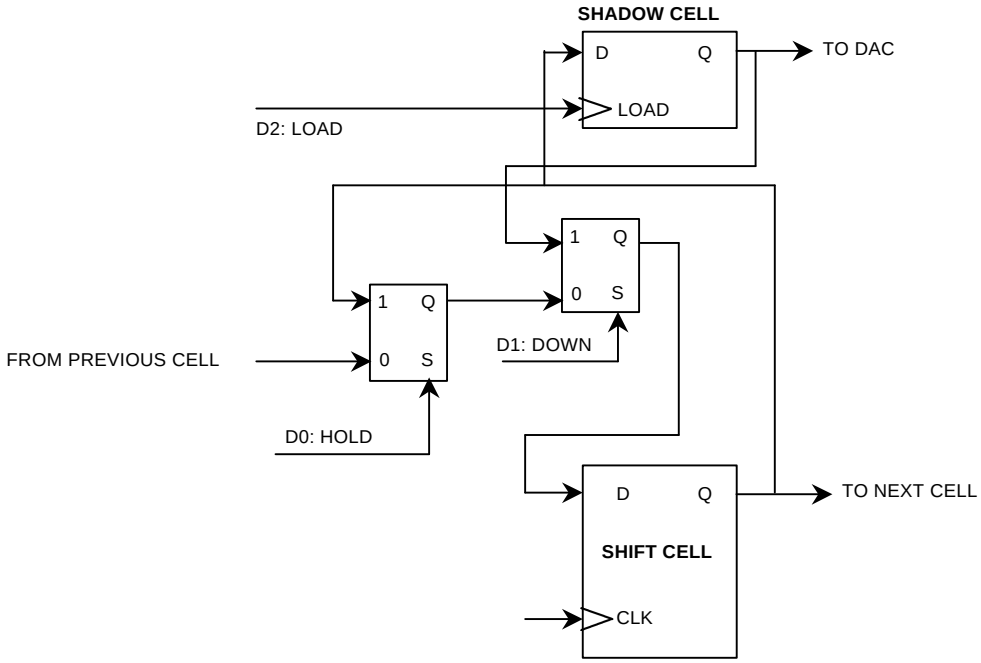

Figure 1. **Serial data interface**

[1] The FPGA may be replaced by an ASIC in the final production version of the MDT readout mezzanine board.

Table 1. **Serial interface signal lines**

DATA_IN	Data line from controller to ASD shift register input
DATA_OUT	Data line from ASD shift register output to controller
CLK	Clock line
D[0:2]	Register control lines

Table 2. **Serial interface instruction encoding**

Instruction	D0	D1	D2	Operation
SHIFT	0	0	X	Shift right at rising edge of CLK
HOLD	1	0	X	Keep shift register contents (self feedback)
DOWN	X	1	X	Copy contents of shadow register to shift register @ rising edge of CLK
LOAD	X	X	1	Load shadow registers with contents of shift register @ rising edge of CLK

Shift and shadow registers have a length of 54 bits, where 53 are actual data bits. The last shift register cell is clocked with an inverted clock, making the output change at the falling edge of the clock. A DOWN instruction causes the last cell to perform a HOLD operation.

The serial data interface was tested up to a clock frequency of 150 MHz. No data corruption was observed. Registers and logic were tested to work within a supply voltage range of 2.0 V to 5.0 V.

Programmable analog parameters

1. Timing discriminator threshold

The threshold for the timing discriminator (DISC1) is applied at the AC coupled input of the pre-comparator differential amplifier (DA-4). As the signal path is fully differential, we use two complementary 8-bit dual resistor divider voltage-DACs (Figure 2) with an output swing of V_{base} ± 128 mV where V_{base} is nominally VDD/2. One of the DACs receives an inverted set of control signals. Consequently the potential difference between both DAC outputs, corresponding to the applied threshold, can vary from 256 mV through zero to –256 mV. The nominal threshold setting is V_{base} ± 30 mV (60 mV effective threshold). Refer to [3][5] for the determination of optimum threshold levels.

Positive and negative reference potentials are supplied by bootstrap type voltage references.

Table 3 summarizes the main design parameters and measurement results of the voltage DAC. The characteristic transfer curve is shown in Figure 3. Differential and integral nonlinearity, the most important DC performance parameters of a converter, are defined in Table 3 and plotted in Figure 4 and Figure 5. Dynamic performance is not critical, yet the DAC was measured to settle to a full-swing step (00000000 → 11111111) within some hundred nano seconds.

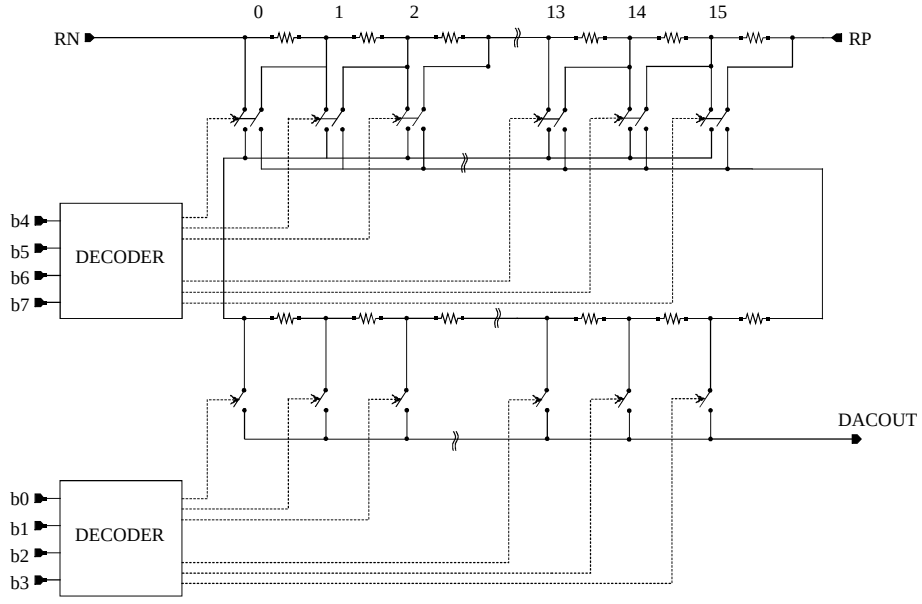

Figure 2. **Block schematic of the 8-bit main discriminator threshold voltage DAC**

Table 3. **Main threshold DAC properties**

Parameter	Definition	Specified	Measured	Units
Type	VDAC	–	–	–
Range	$V_{RP} - V_{RN}$	256	256	mV
Resolution	N bits	8	–	–
LSB	$(V_{RP} - V_{RN})/2^N$	1	1	mV
Differential nonlinearity	$MAX(V_{n+1} - V_n) - LSB$	< 1	0.7	mV
Integral nonlinearity	$MAX(V_n - V_{n,ideal})$	< 5	3.2	mV
Monotonicity	$V_n \leq V_{n+1}\ \forall\ n$	–	**Ö**	–
No Missing code	$V_n \neq V_{n+i}\ \forall\ n, i$	–	**Ö**	–

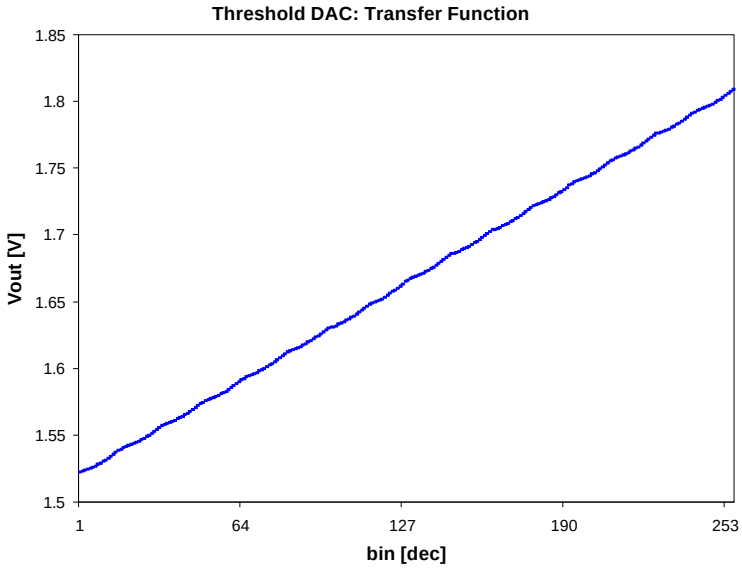

Figure 3. **VDAC transfer function**

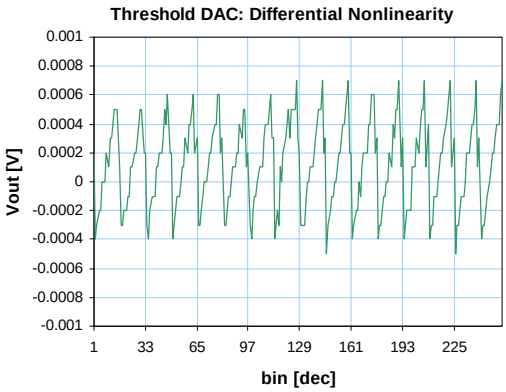

Figure 4. **VDAC differential nonlinearity**

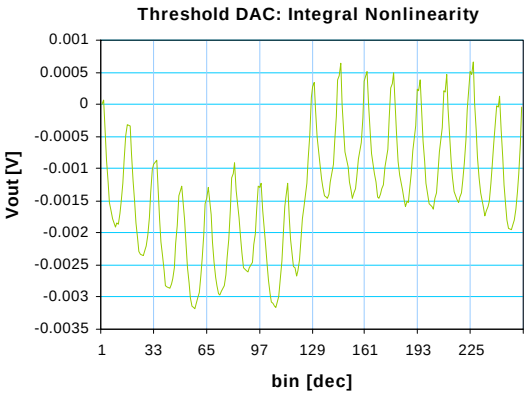

Figure 5. **VDAC integral nonlinearity**

2. Timing discriminator hysteresis

It was demonstrated that the option of a wide-range adjustable hysteresis for the timing discriminator is a useful feature to reduce the probability of multiple threshold crossings in the tail of the MDT signal [5]. It also improves the system reliability by removing ambivalent output states of the comparator due to signals or signal fluctuations close to the threshold level.

The hysteresis for DISC1 is applied through a scaled-transistor current source DAC with a resolution of 4 bits. The range of the DAC is 30 µA with a LSB of 1.875 µA. This corresponds to a hysteresis voltage range of 0 – 20mV at the threshold coupling point DA–4 (0 – 7 primary electrons) or 0 – 100mV at the comparator.

A direct measurement of the hysteresis voltages is not feasible, though the functionality was assessed qualitatively. The linearity of the current DAC can be derived from a measurement of the shift in effective threshold voltage and the subsequent delay in discriminator action (Figure 6).

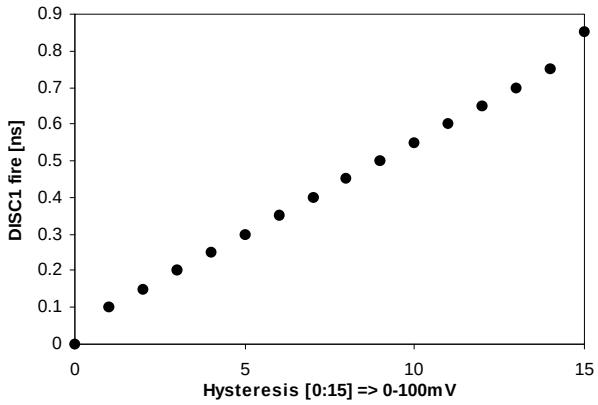

Figure 6. **Discriminator action vs. hysteresis voltage setting, yielding hysteresis current DAC linearity**

3. Wilkinson ADC Control

The purpose of the Wilkinson ADC is to provide data which can be used for the correction of time-slew effects (Figure 7) by measuring the charge contained in the rising edge of the MDT signal [3][5][6]. In addition, this kind of charge measurement provides a tool useful for chamber performance diagnostics. Further applications such as *dE/dx* measurements etc are conceivable.

The result of the charge measurement is converted into time, encoded in the width of the output pulse (pulse width encoding). The information contained in the pulse, namely the leading edge timing and the pulse width encoded charge, can be read and converted to digital data by a TDC [7].

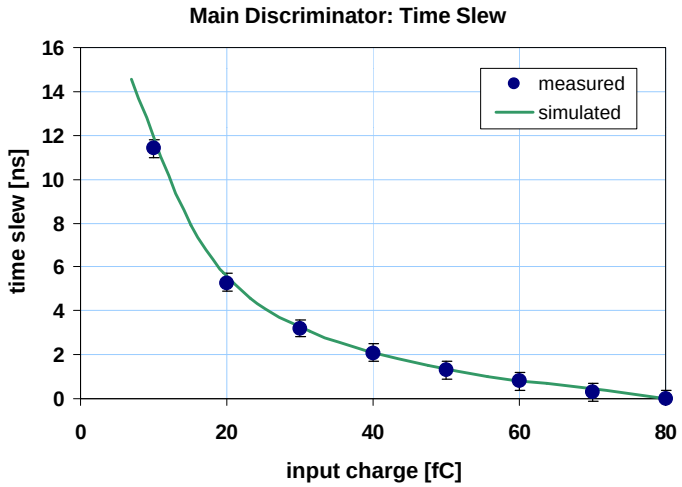

Figure 7. **Measured and simulated time slew of the MDT-ASD signal chain. The slew is the timing of the discriminator 50% point of transition as a function of input signal amplitude relative to the timing of a maximum amplitude signal (in this case a 80 fC signal).**

4 parameters of the Wilkinson ADC are controllable: the integration gate width, the discriminator threshold, the discharge current and the deadtime.

- The **integration gate width** can be set from 11 ns to 35 ns in steps of 1.5 ns (4-bit). This setting influences what fraction of the leading edge charge of the signal is used for time slew correction. The nominal gate width is 15 ns which corresponds to the average peaking time t_p of the preamp pulse. It can be demonstrated that the time slewing is only correlated to the leading edge charge and not to the total signal charge of the MDT signal. ADC measurements with a gate $> 2 \times t_p$ thus can not be used to further improve the spatial resolution of the system [3][5].

- The **threshold** is applied to the differential threshold terminals of the Wilkinson discriminator (DISC2) by two coupled resistor divider voltage DACs with 3-bit resolution and a range of 16 mV to 128 mV (LSB = 14 mV). One set of control signals sets both DACs complementary. Unlike DISC1 threshold, the two DACs do not cover the same range. The positive range is V_{base} + 16 mV to V_{base} + 128 mV, the negative from V_{base} – 16 mV to V_{base} – 128 mV. The minimum threshold thus amounts to 32 mV. The same voltage references as for the DISC1 threshold DACs are used. The DISC2 threshold also affects the width of the Wilkinson ADC output pulse (see below) but does not influence the ADC performance in a wide range and is primarily implemented for troubleshooting and fine tuning purposes.

- The **discharge current** of the integration capacitors is set by a switched resistor chain in a range between 1 µA and 2.5 µA (3-bit). This allows the ADC output pulse width to be adjusted to the dynamic range of the TDC (200 ns @ resolution 0.78125 ns). This pulse width range (caused by the MDT signal amplitude range) is jointly determined by the integration gate width, the DISC2 threshold and the discharge current. For nominal settings (integration gate: 15 ns, DISC2 threshold: 32 mV complimentary) and a typical input signal, the ADC output can be set between 85 ns and 135 ns by controlling the rundown current. The nominal setting (1.4 µA) yields a 110 ns output pulse. The dynamic range (input signal from "just-above-threshold" to saturation) of the ADC output appears at these nominal settings to be 40 ns – 140 ns (100 ns range ⇒ 7-bit TDC resolution). See Figure 9 for simulated Wilkinson ADC performance.

- The **deadtime** setting defines an additional time window after each hit in which the logic does not accept and process new input. It can be set from 300 to 1100 ns in steps of 100 ns (3 bit). The nominal setting is 800 ns corresponding to the maximum drift time in the MDT. This feature can be used to suppress spurious hits due to multiple threshold crossings in the MDT signal tail (additionally facilitated by the bipolar shaping scheme).

  The deadtime window is added to the output pulse, thus a minimum deadtime is always present (the time of the output pulse itself).

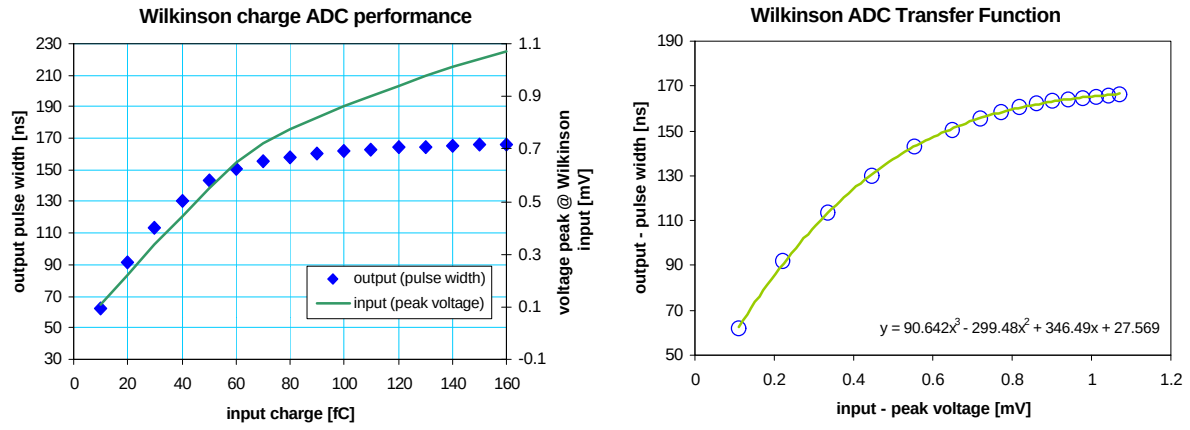

Figure 8. **Spice simulation/measurement of Wilkinson ADC characteristics. The left-hand plot shows the width of the output pulse (simulated) and peak voltage at the ADC input (simulated and measured) as a function of the input signal charge. Consequently this plot includes both the nonlinearities of the amplifier chain and the converter. It has to be noted is that the plots cover a greatly extended input signal range. The expected working range will be in the area of ~ 20 - 80 fC. The right-hand plot shows the converter transfer characteristic (ADC output vs. input). All simulations/measurements were taken with the following parameter settings: Integration gate 17 ns, DISC2 threshold 64 mV, discharge current 1.6 mA.**

Different combinations of the ADC settings affect the output pulse in a wide range. For minimum integration gate (11 ns), high rundown current (2.5 μA) and high DISC2 threshold (128mV), the width of the pulse can go as low as 15 ns for a very small input signal. The other extreme (gate 34 ns, rundown current 1μA, DISC2 threshold 16 mV) yields a 240 ns ADC output pulse for a large signal (note that at certain settings, the TDC dynamic range can be exceeded!). Figure 9 shows the ADC output pulse width for three different integration gate settings as functions of the rundown current. The output pulse widths lie within the shaded areas depending on input signal charge and rundown current setting.

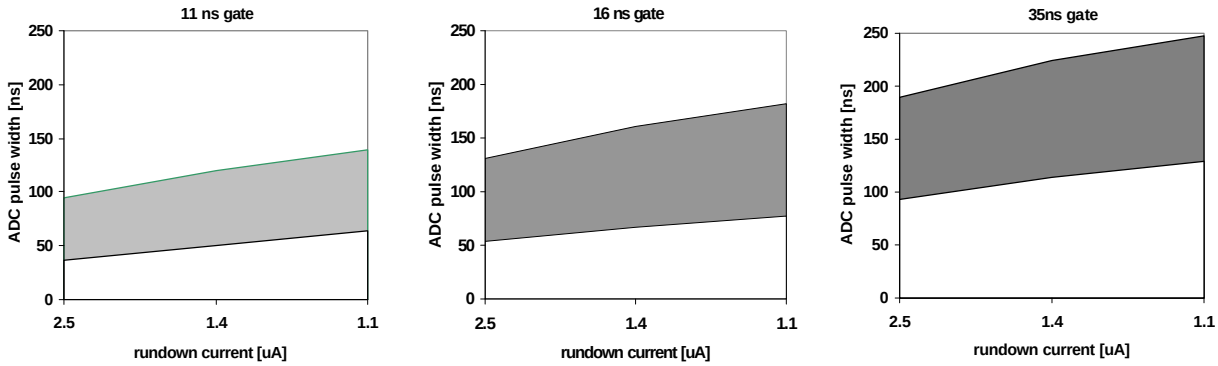

Figure 9. **Influence of integration gate and rundown current settings on the ADC output pulse width.**

Programmable functional parameters

1. Calibration/test pulse injection

In order to facilitate chip testing at the design stage as well as to perform system calibration and test runs in the final assembly, a calibration/test pulse injection system was integrated in the chip. It consists of a parallel bank of 8 switchable 50 fF capacitors and an associated channel mask register. The mask register allows for each channel to be selected separately whether or not it will receive test pulses. The on-chip capacitors are charged with external voltage pulses, nominal 200 mV swing standard LVDS pulses, yielding an input signal charge range of 10 – 80 fC. Figure 10 shows the voltage of the analog output pulse peak versus input charge using the calibration injection system. The discrepancy between simulation and measurement is marginal. It can be caused by various effects, including variations of process parameters. Measurement results assuming the calibration capacitors being 10% below designed value are added for illustration (solid blue line).

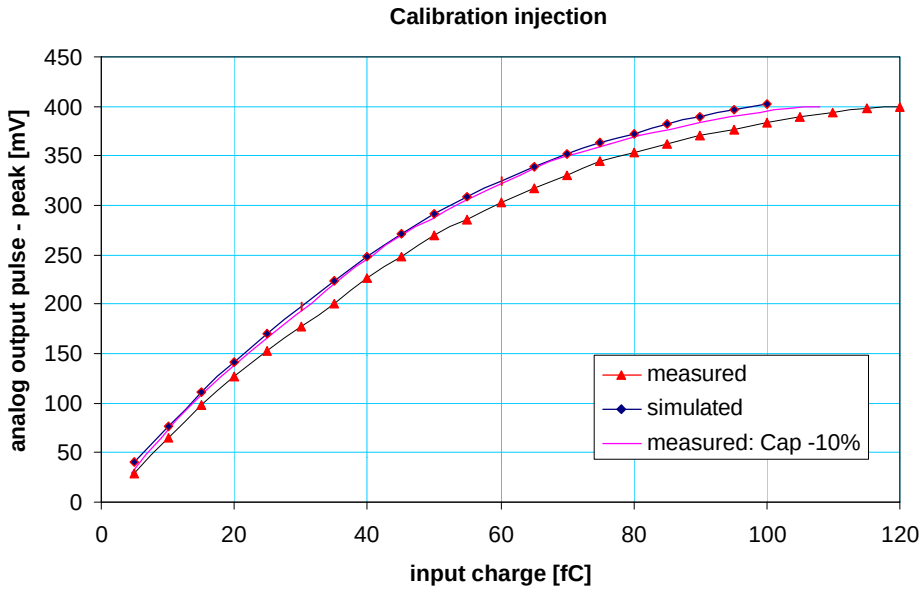

Figure 10. **Simulated and measured analog output pulse peak versus input charge using the calibration injection system. The blue solid line represents measurement results assuming the on-chip calibration capacitors being 10% lower than their designed value.**

2. Chip mode

One bit is used to set the global output mode of the MDT-ASD. The two modes are:

Mode	Description
ADC mode (default)	In this mode, the output pulse width represents the charge measured in the leading edge of the MDT signal (pulse width encoded charge measurement, see section "Wilkinson ADC control"). The rising edge contains the timing information.
TOT mode (Time-over-Threshold)	In this mode, the discriminator signal itself is sent to the output drivers. Thus the width of the pulse is determined by the shape and amplitude of the MDT signal. Multiple threshold crossings (and output pulses) are possible. The rising edge of the first (main) pulse contains the timing information for the event.

3. Channel mode

For diagnostic (boundary scan) and troubleshooting purposes, the output of each channel can be set to one of the four states (2 bits per channel):

State	Description
ACTIVE	Channel on. Default working setting.
HIGH	LVDS output of the respective channel is always 'Logic 1' (regardless of what happens in the analog part of this channel).
LOW	Like above but 'Logic 0'. These two settings allow boundary scan type connectivity checking of the circuit board. Particularly useful for large scale production testing.
OFF	The preamp of the respective channel is disabled. This is a troubleshooting feature that allows single channels to be turned off in case of oscillations etc. The LVDS output of the channel is set to '0'.

Data format and protocol

Table 4 gives a summary of all programmable parameters including their nominal/default settings, the range, resolution/LSB and number of bits. The total number of control bits/ASD chip is 53. A power-up/reset routine, which loads the ASD registers with the nominal values of Table 4. will be incorporated in the JTAG controller[2].

The bit assignment of the shift register is given in Table 5. JTAG bit 0 is the last bit to enter the shift register. Data words are loaded LSB first. Channel 1 is the top most channel when looking at the chip with the analog inputs at the left-hand side. The mask bit for channel 1 is JTAG bit 0.

Table 4. **Summary of programmable parameters**

Parameter	Nominal value	Range	LSB	Units	Resolution	bit
DISC1 Threshold	60	0 – 256	1	mV	256	8
DISC1 Hysteresis	10	0 – 20	1.25	mV	16	4
Wilkinson integration gate	15.5	11 – 35	1.5	ns	16	4
DISC2 Threshold	30	16 – 128	14	mV	8	3
Wilkinson discharge current	1.4	1 – 2.5	0.1875	μA	8	3
Deadtime	800	300 – 1100	100	ns	8	3
Calibration channel mask	–	–	–	–	–	8
Calibration capacitor select	–	50 – 400	50	fF	8	3
Channel mode	ACTIVE	–	–	–	–	16
Chip mode	ADC	–	–	–	–	1

Total number of bits: 53

[2] There exists also the option to implement this feature on the ASD chip itself.

Table 5. **Shift register bit assignment**

JTAG bit #	Description	LSB/code
[0:7]	Channel mask register 1 – 8 [0:7]	bit 0 channel 1 (top)
[8:10]	Calibration injection capacitor select [2:0]	bit 10 LSB
[11:18]	Main threshold DAC (DISC1) [7:0]	bit 18 LSB
[19:21]	Wilkinson ADC threshold DAC (DISC2) [2:0]	bit 21 LSB
[22:25]	Hysteresis DAC (DISC1) [3:0]	bit 25 LSB
[26:29]	Wilkinson ADC integration gate [3:0]	bit 29 LSB
[30:32]	Wilkinson ADC rundown current [2:0]	bit 32 LSB
[33:35]	Deadtime [2:0]	bit 35 LSB
[36:37]	Channel mode – channel 1 (top) [1:0]	‘00’ ACTIVE ‘01’ HIGH ‘10’ LOW ‘11’ OFF
[38:39]	Channel mode – channel 2 [1:0]	
[40:41]	Channel mode – channel 3 [1:0]	
[42:43]	Channel mode – channel 4 [1:0]	
[44:45]	Channel mode – channel 5 [1:0]	
[46:47]	Channel mode – channel 6 [1:0]	
[48:49]	Channel mode – channel 7 [1:0]	
[50:51]	Channel mode – channel 8 (bottom) [1:0]	
[52]	Chip mode	‘0’ ADC, ‘1’ TOT

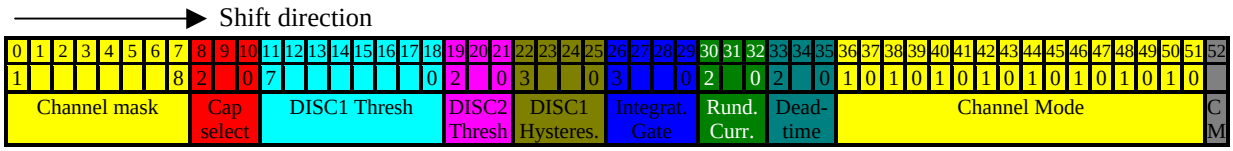

Figure 11. **Shift register image**

Appendix

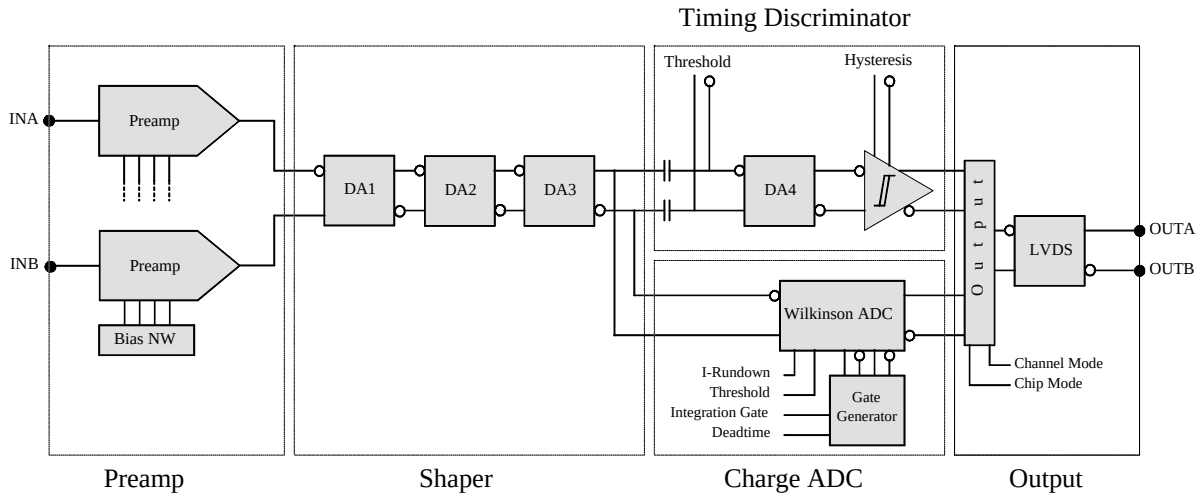

Figure 12. **MDT-ASD channel: Block schematic**

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