# MDT-ASD: LVDS driver properties

The characteristics of the MDT-ASD LVDS-drivers on an ASD99D were assessed according to the specifications in the IEEE P1596.3 (LVDS) standard document.

## 1. Driver DC specifications

Table 1 gives the LVDS "reduced range link" driver DC specifications for a nominal 100 Ω termination and results from measurements at a power supply voltage of 3.3 V. All measurement results lie within the specifications at nominal conditions.

Table 1. **LVDS "reduced range link": Driver DC specifications and MDT-ASD LVDS driver properties measured at $V_{sup}$= 3.3V**

| Symbol | Parameter | Conditions | Min | Max | Measured | Units |
|---|---|---|---|---|---|---|
| $V_{oh}$ | Output voltage high, $V_{oa}$ or $V_{ob}$ | $R_{load}$ = 100 Ω ± 1% | | 1375 | 1335 | mV |
| $V_{ol}$ | Output voltage low, $V_{oa}$ or $V_{ob}$ | $R_{load}$ = 100 Ω ± 1% | 1025 | | 1165 | mV |
| $\|V_{od}\|$ | Output differential voltage | $R_{load}$ = 100 Ω ± 1% | 150 | 250 | 170 | mV |
| $V_{os}$ | Output offset voltage | $R_{load}$ = 100 Ω ± 1% | 1150 | 1250 | 1250 | mV |
| $R_0$ | Output impedance, single ended | $V_{cm}$ = 1.0V and 1.4V | 40 | 140 | - | Ω |
| $\Delta R_0$ | $R_0$ mismatch between a & b | $V_{cm}$ = 1.0V and 1.4V | | 10 | - | % |
| $\|\Delta V_{od}\|$ | Change in $\|V_{od}\|$ between `0` and `1` | $R_{load}$ = 100 Ω ± 1% | | 25 | 2 | mV |
| $\Delta V_{os}$ | Change in $V_{os}$ between `0` and `1` | $R_{load}$ = 100 Ω ± 1% | | 25 | 1 | mV |
| $I_{sa}$, $I_{sb}$ | Output current | Driver shorted to ground | | 40 | 3.7 | mA |
| $I_{sab}$ | Output current | Drivers shorted together | | 12 | 1.5 | mA |

Figure 1 shows the variation of the driver dc levels as a function of the power supply voltage VDD. The upper voltage level $V_{oh}$ remains below the specified maximum up to a VDD of 3.42V. The lower voltage level $V_{ol}$ remains above the specified minimum down to a VDD of 2.9V. The output offset voltage $V_{os}$ stays within the specified range for a VDD between 3.0V and 3.3V.

Figure 2 shows the dependency of the driver output differential voltage $V_{od}$ on the power supply voltage VDD. $V_{od}$ lies within the specified range from VDD = 3.17V to VDD well above 3.6V.

**Driver DC levels** are measured to lie within the LVDS reduced range link standard specification for a power supply voltage variation from **3.17 V to 3.3 V ($VDD_{nom}$ - 4% to $VDD_{nom}$ + 0%) at nominal termination (100 W).**

Figure 3 and Figure 4 show the variation of the driver dc levels as a function of the power supply voltage for a termination resistance $R_{load}$ = 200 Ω. $V_{oh}$ exceeds the upper limit at VDD = 3.22 V, $V_{os}$ stays in range from 3 V to 3.44 V, $V_{ol}$ from 3.05 upwards.

The variation of the driver output differential voltage $V_{od}$ as a function of load resistance is shown in Figure 5. $V_{od}$ remains within the specified limits for $R_{load}$ from 90 Ω to 150 Ω at VDD = 3.3V.

$\Delta V_{os}$, the change in output offset voltage between `0` and `1` is shown in the bottom oscilloscope trace of Figure 6. $V_{oa}$ and $V_{ob}$ are represented by the top traces labeled 1 and 2. The amplitude cursor yields a difference of 2 mV. This number has to be divided by 2 according to $V_{os} = (V_{oa} + V_{ob})/2$, yielding the value of 1 mV in Table 1. $|\Delta V_{od}|$ was measured in a similar way (compare Figure 9).

The short-circuit output currents $I_{sa}$, $I_{sb}$ and $I_{sab}$ were measured according to the definitions in the LVDS standard document.

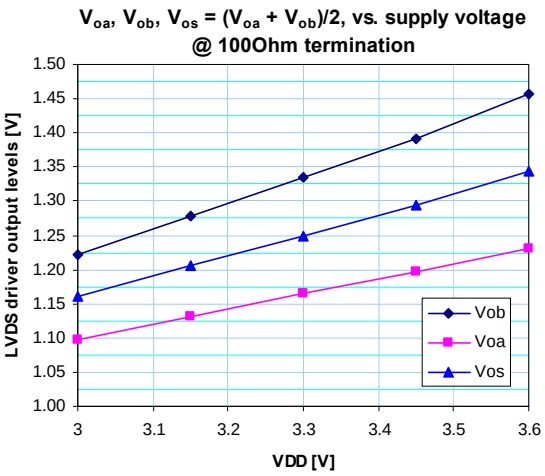


Figure 1. **Driver levels vs. supply voltage**

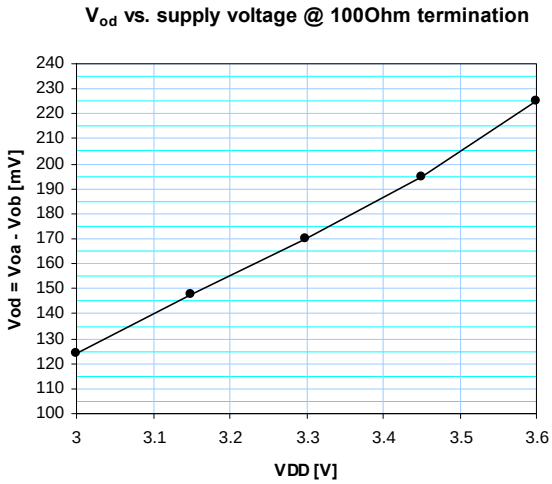


Figure 2. **Driver differential voltage vs. supply voltage**

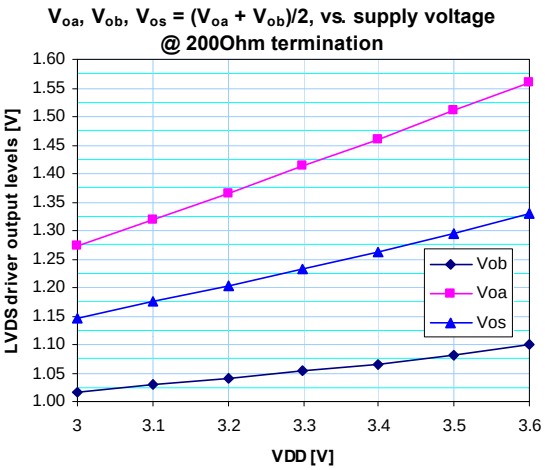


Figure 3. **Driver levels vs. supply voltage @ 200 W**

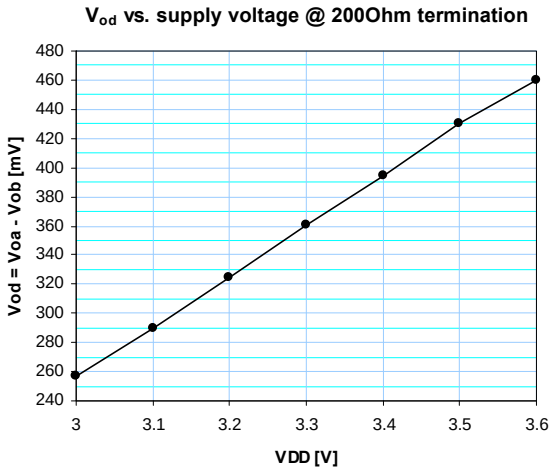


Figure 4. **Driver differential voltage vs. supply voltage @ 200 W**

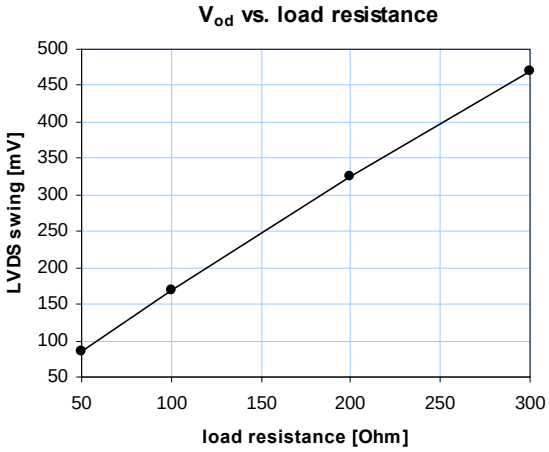


Figure 5. **Driver differential voltage vs. load resistance**

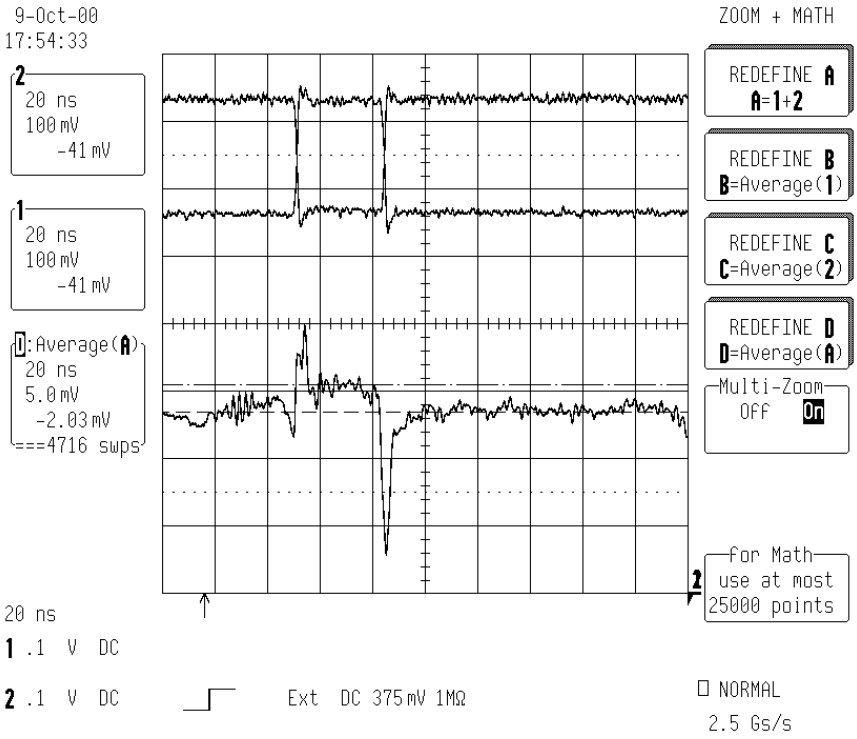


Figure 6. **$DV_{os}$ - change in output offset voltage $V_{os}$ between `0` and `1`**

## 2. Driver AC specifications

The LVDS standard document specifies AC parameters for clock and data signals. Relevant for MDT-ASD are rise- and fall-time and differential skew, while clock signal duty cycle and channel-to-channel skew are not applicable. Table 2 gives the LVDS driver AC specifications for a nominal 100 Ω termination and results from measurements at a power supply voltage of 3.3 V. Rise- and fall-time (Figure 8) exceed the specifications by a factor of 2, skew (Figure 10) lies well within specs. The measurements were done under conditions illustrated in Figure 7.

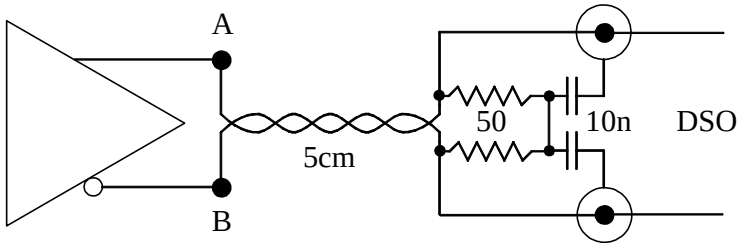


Figure 7. **Connection setup: 5cm twisted pair terminated with 50 W resistors, 10nF caps to scope ground.**

Table 2. **LVDS Driver AC specifications and MDT-ASD LVDS driver properties measured at $V_{sup}$= 3.3 V**

| Symbol | Parameter | Conditions | Min | Max | Measured | Units |
|---|---|---|---|---|---|---|
| $t_{fall}$ | $V_{od}$ fall time, 20% to 80% | $Z_{load}$ = 100 Ω ± 1% | 300 | 500 | 940 | ps |
| $t_{rise}$ | $V_{od}$ rise time, 20% to 80% | $Z_{load}$ = 100 Ω ± 1% | 300 | 500 | 970 | ps |
| $t_{skew}$ | Differential skew<br>$\|tp_{HLA} - tp_{HLB}\|$ or $\|tp_{HLB} - tp_{HLA}\|$ | Any differential pair,<br>@ 50% point of transition | | 50 | 20 | ps |

Measurements in Figure 8 and Figure 9 were taken at a test pulse frequency of 25 MHz. No high rate effects are observable. Figure 8 gives rise- and fall-times $t_{rise}$ and $t_{fall}$, the output differential voltage $V_{od}$ (ampl) and the output offset voltage $V_{os}$ (median), Figure 9. yields $|\Delta V_{od}|$.

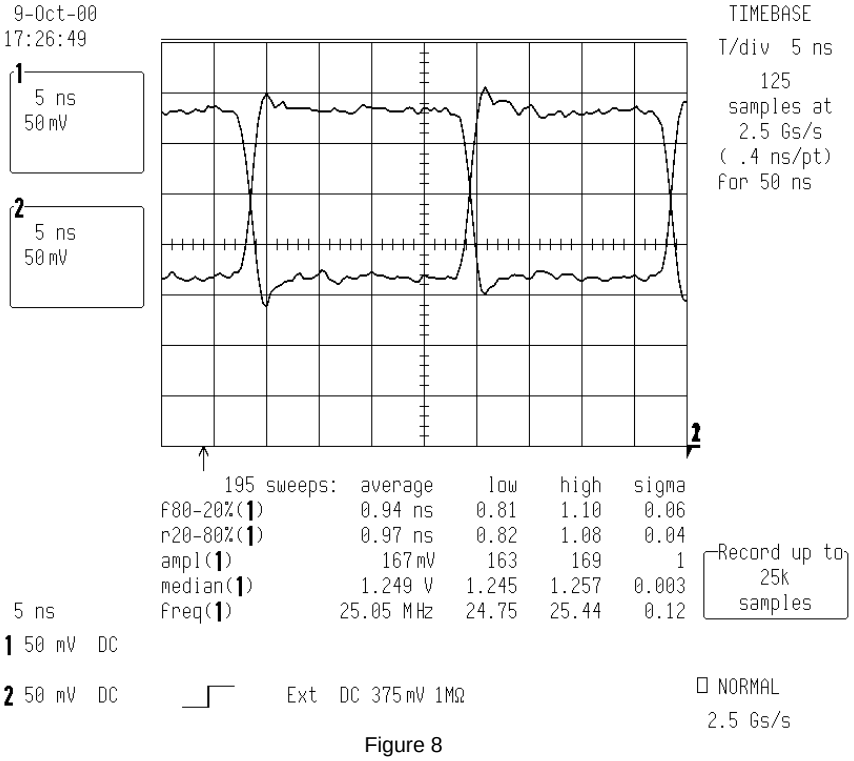


Figure 8

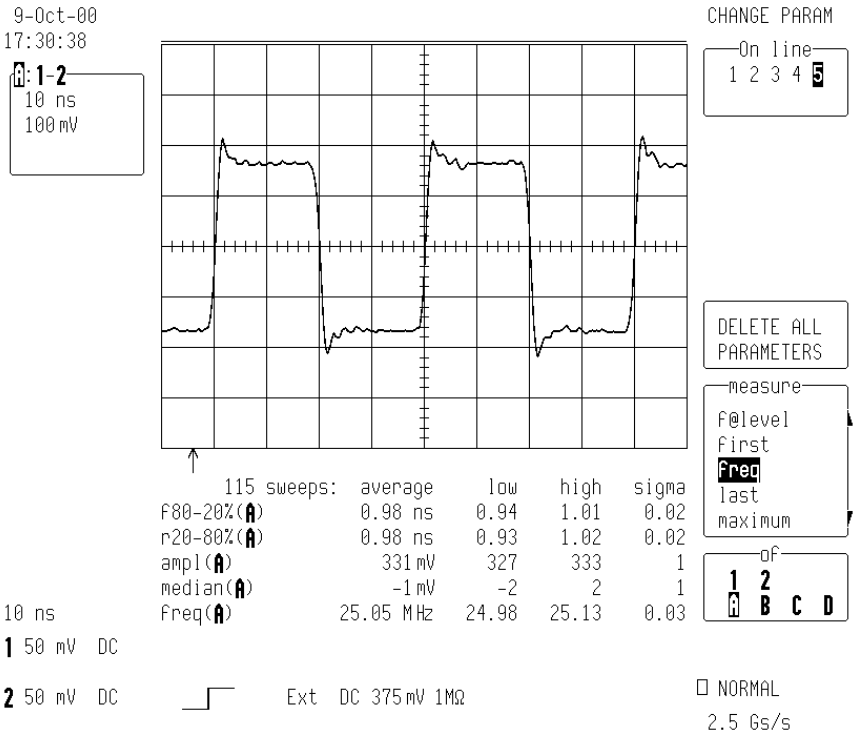


Figure 9. **$|\Delta V_{od}| = 2\ |\text{median}(A)| = 2$ mV**

The skew measured in Figure 10 is the time difference between the high-to-low and low-to-high transitions of complementary single ended channels. The measured value of 20 ps is well below the specified maximum of 50 ps.

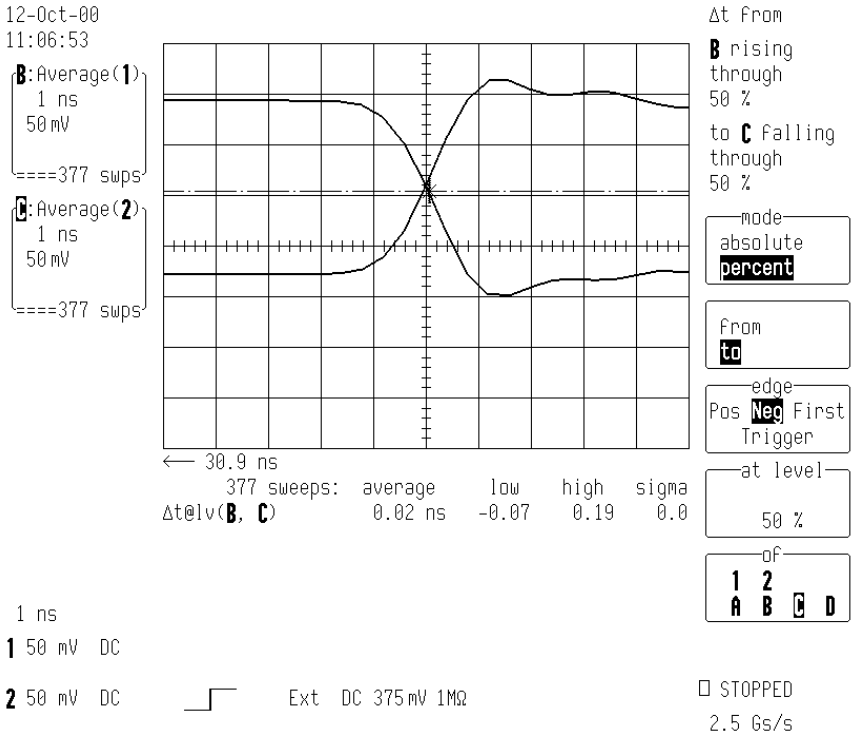


Figure 10. **Skew: 20 ps**

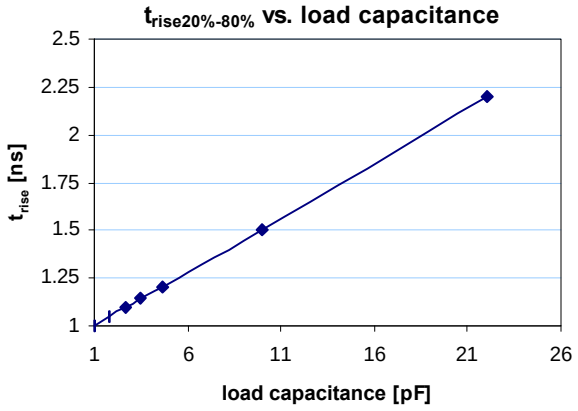


Figure 11

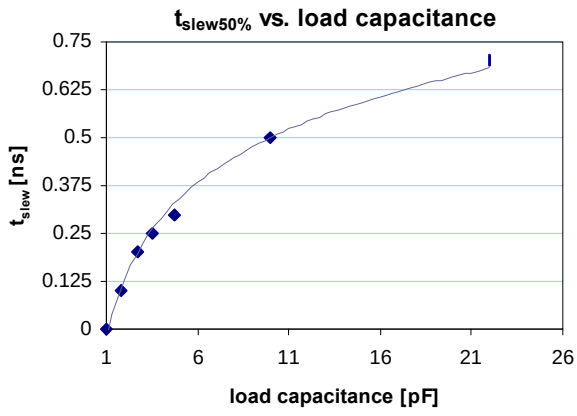


Figure 12

Figure 11 shows the increase of $t_{rise}$ as a function of the load capacitance. Time slew measured at $V_{os}$ versus load capacitance is shown in Figure 12.

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Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE P1596.3-1995 standard document.