ATLAS MDT Front End Chip
DRAFT
Specification

22 January, 1998

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1. Introduction

This note serves as a specification for the ATLAS Muon front end readout chip. It describes its general features, modes of operation, analog specifications, and digitally programmable parameters. Its main function is to serve as a guide for prototype chip submissions and does not constitute a complete description of MDT on-chamber electronics in general. It is anticipated that this document will be updated from time to time to reflect recent changes and detailed design decisions.

The ASD development will proceed in two distinct stages. The first is the production of a simplified four channel ASD chip referred to as "**ASD-Lite**" intended for application in early MDT chamber tests. This device, to be described more fully in subsequent sections, will have no programmable features and hence, no digital interface. It is a dedicated device intended for simple time-over-threshold measurements with some programmability provided by externally adjustable bias currents.

The final device is the eight channel "**MDT_ASD**". It will have full digital i/o for accessing programmable register locations to which operating constants may be downloaded. These constants, to be described more fully in later sections, are for the setting of various modes of operation, bias currents and voltages, tail cancellation shaping time constants, and discriminator threshold levels.

2. General features

The general analog features of each channel are shown in the block diagram below and described in more detail in later sections. Some features pertain to both ASD-Lite and MDT-ASD while some pertain only to the latter.

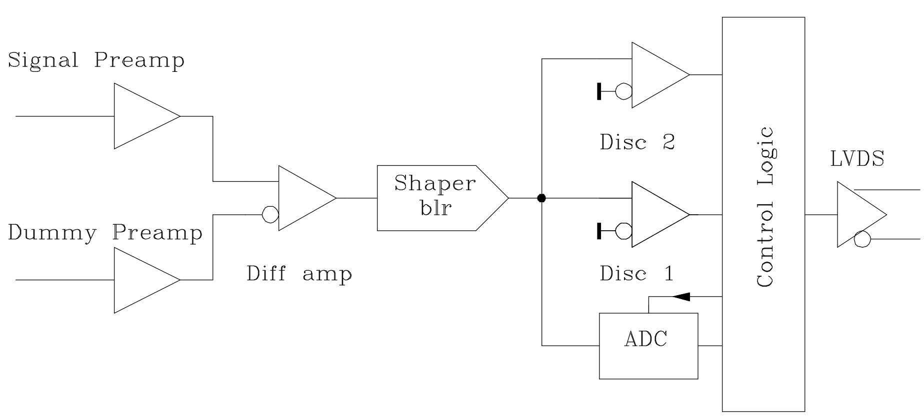


Figure 1

2.1 CMOS Process

The ASD chip development is proceeding in Hewlett Packard's 0.5 micron n-well CMOS process provided through the MOSIS service. This process is characterized for operation at 3.3 volts but may be used up to 5.0 volts for some structures. The MDT-ASD is designed for operation at 3.3 volts.

2.2 Preamplifier

The input stage is referred to as pseudo-differential consisting of two identical transimpedance amplifiers. One preamp, the *signal preamp*, is connected to the MDT through a trace on the hedgehog printed circuit board and a high voltage decoupling capacitor. The other, or *dummy,* preamplifier is connected to a trace which runs parallel to the signal trace but is otherwise unconnected to the chamber. Its purpose is to provide dc balance to the shaper and subsequent stages, but more importantly, to provide common mode rejection to pickup, crosstalk, and noise on the power supply lines. The preamplifier schematic is shown below in Fig 2.

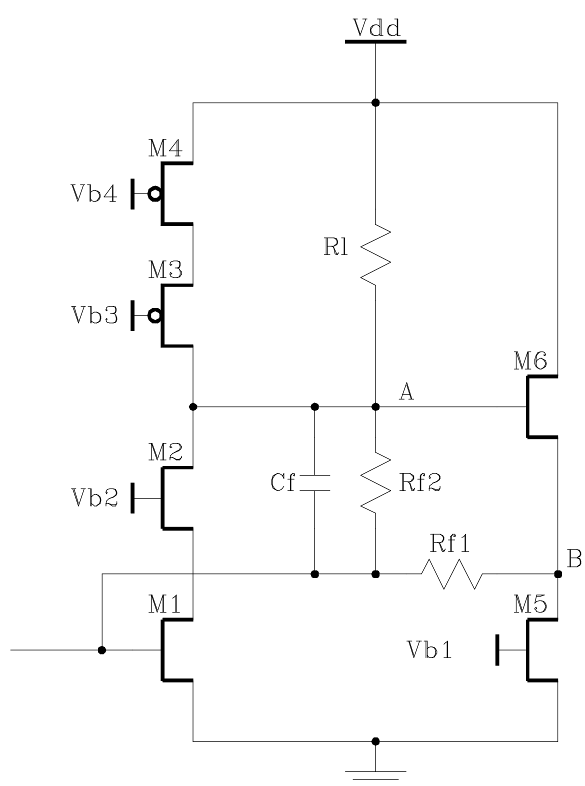


Figure 2

It is an unfolded cascode with main gain transistor M1. At present, M1 is 2400u/0.9u but may be longer in subsequent versions. It operates in medium to weak inversion depending on the transistor's size and its operating current. M2 forms the cascode for M1 while M3 and M4 form a high impedance cascode current source. Operation at 3.3 volts requires input transistors and current source transistors to operate at extremely low "overhead". Thus M1, M5, and M4 operate with drain-source voltages of order 0.3 to 0.4 volts. A global bias circuit (not shown) provides the required bias voltages Vb1-Vb4.

The input impedance of the preamplifier (at high frequencies) is given by

$$Z_{in} = \frac{1}{G_{m1}} \cdot \left(1 + \frac{C_{stray}}{C_f}\right)$$

Zin is thus governed by the transconductance of M1 which in turn, depends on its size and operating current. Thus input impedance improves with operating current but is degraded by stray capacitance at the high impedance node (source/drain of M3/M2). Design goal is for Zin of 100 Ohms at operating current of 1ma, or 3.3 mW per preamp.

2.3 Shaper

The shaper is a two stage pole/zero filter which cancels the long positive ion tail on the MDT signal. It also provides additional gain beyond that of the preamplifier. Its gain is chosen so that the entire dynamic range of MDT signals is within the linear region of operation for a fixed gas gain. Its basic topology is shown below.

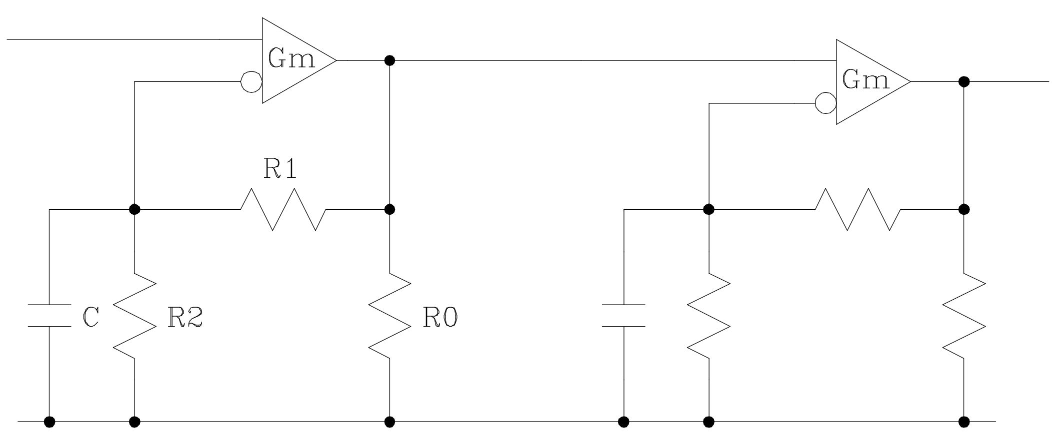


Figure 3

Preceding the shaper, there is a simple differential amplifier (not shown) which takes the difference of the signal and dummy inputs and presents it to the shaper. Each stage of the shaper provides a pole/zero function as follows.

For high frequency components, the gain of each stage is simply the product of Gm x R2. At these frequencies, there is no feedback and in that sense it is open loop. This feature makes optimal use of available transistor gain-bandwidth and provides short peaking time. Each shaper stage contributes of order 2-3 ns to the peaking time with a gain of approximately four. For lower signal frequencies, the voltage divider R0, R1 along with C0 provides feedback to the negative input, thus reducing the gain at these frequencies. Thus a pole/zero network is formed with the pole/zero ratio given by the ratio of closed loop gain at high frequency divided by that at lower frequency.

The pole and zero locations and ratios are determined using the "industry standard" prescription [[1]]

$$T_{Z1} = 113 \cdot t_0, \qquad T_{p1} = 70 \cdot t_0, \qquad T_{Z2} = 13.5 \cdot t_0, \qquad T_{p2} = 5.4 \cdot t_0$$

where t_0 is the characteristic time associated with positive ion drift in a circular drift tube. In the above realizations, assuming $R_1, R_2 << R_0$, the resistor ratio is determined by

$$\frac{R_1}{R_2} = \frac{G_m \cdot R_0}{n-1} - 1$$

where

$$n = \frac{T_z}{T_p}$$

is the ratio of the zero to pole time constants for that stage. The capacitor is then determined by

$$C = T_z \cdot \frac{R_1 + R_2}{R_1 \cdot R_2}$$

In practice, various tradeoffs are used to determine reasonable values for the passive components. In particular, capacitors in excess of 100pf and resistors in excess of 100k tend to be unwieldy in the HP 0.5 micron technology. Fortunately, this leaves ample room for choosing reasonable components.

2.4 Baseline Restoration

At the time of this writing, an active baseline restoration implementation is under investigation for inclusion in the ASD. In this technique, an amplifier samples the voltage at the output of the shaper, performs some analog signal processing (to be

[1] Boie, Hrisoho,& Rehak NIM 192 (1982) 356

described), and produces a feedback signal which drives this voltage to a preset level. The overall topology is shown below in Figure 4.

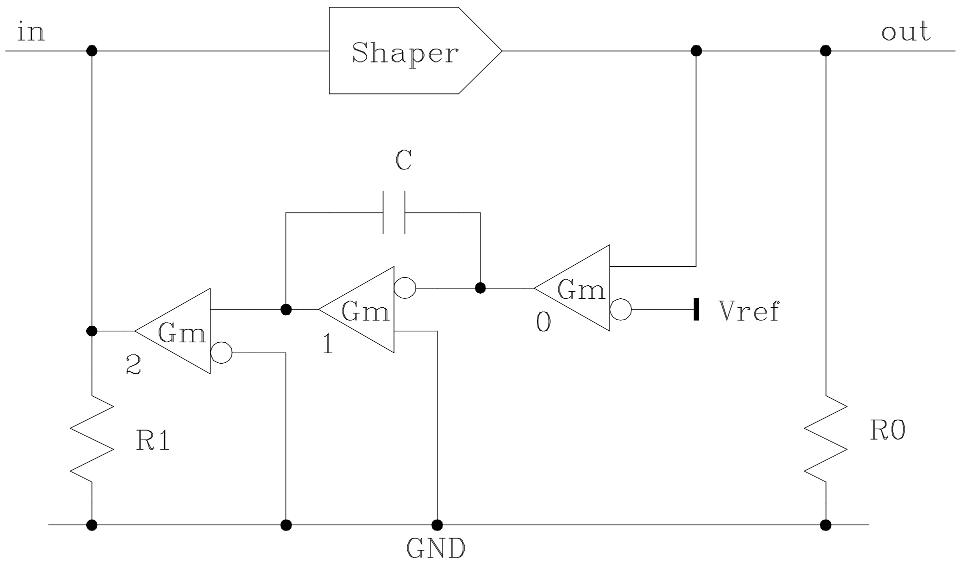


Figure 4

Loop analysis of this topology shows that, assuming linearity, the output node will always be driven to the reference voltage, Vref, with a characteristic time constant given by

$$\tau = \frac{C}{Gm_0 \cdot Gm_2 \cdot R_1}$$

By adjusting the transconductances Gm_0 and Gm_2 (via bias current adjustments), one can tune the response time to a desired value. Thus for linear circuit elements, the closed loop behavior is identical to that of a simple RC coupled stage with time constant τ. It is anticipated that this value will be in the range of approximately 1 to 10 microseconds. If the longer time constant is chosen, then the network has minimal impact on the shape of the pulse. If the shortest time constant is chosen, the network behavior is more similar to bipolar shaping.

To accommodate high rate operation, one must drive the averaged output to the reference voltage in such a way as to ignore excursions above the baseline due to large pulses. In this way, the baseline rather than the signal average is kept at or near Vref, thus eliminating or reducing baseline shift. This requires that Gm0 have a transfer curve which is non-linear.

2.4.1 Non-linear transconductor

A CMOS implementation of the non-linear transconductor is shown in the schematic of Figure 5.

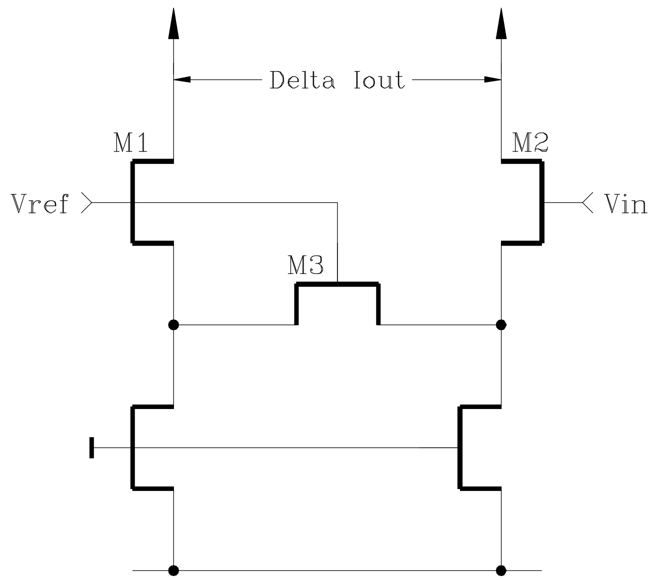


Figure 5

For small excursions of the input signal about the reference voltage, the circuit acts as a linear transconductor with transistor M3 in the triode (resistive) region. The circuit remains quite linear for large negative excursion of Vin where M3 remains in the resistive region. For large positive excursions, M3 saturates and the stage gain goes to zero. Thus the circuit acts as a clipping network and ignores large positive input signals. The level at which the clipping takes place is controlled by the relative sizes of M3 and M1. This circuit is essentially a variation of a linear transconductance cell commonly used in transconductance-C filters. In the latter case, a linear cell is formed by providing a mate to M3 with its gate tied to the gate of M2.

2.5 Discriminator

The discriminator schematic is shown in Figure 6.

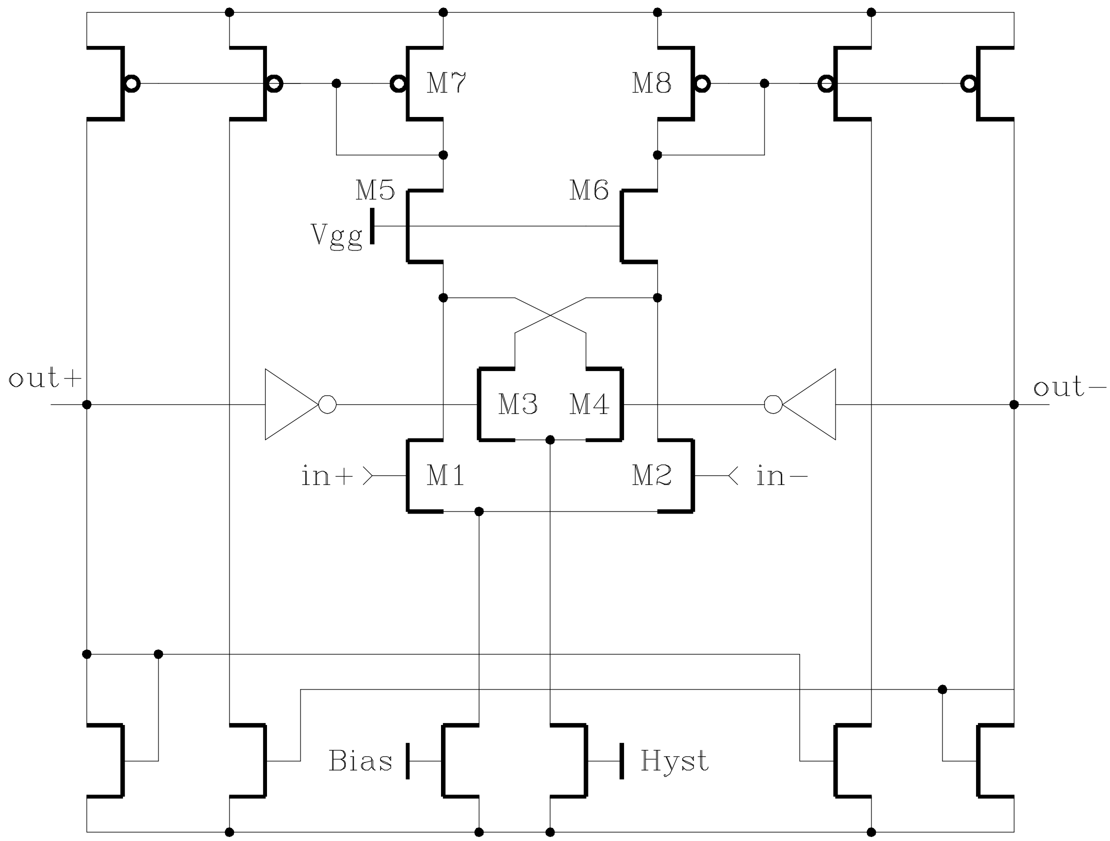


Figure 6

The circuit is a high-gain differential pair M1/M2 with diode-connected loads M7/M8 and tail (bias) current provided from an external input via a 1:1 mirror (not shown). Miller capacitance in M1/M2 is reduced by cascode devices M5/M6. Symmetrical class A/B output stages are provided using two sets of current mirrors. Positive feedback is provided via two inverters and a second differential pair M3/M4 The amount of hysteresis may be programmed externally via current mirror connected to “Hyst”. A primary design goal was to achieve a completely symmetrical design (in both circuit topology and layout) to minimize input offsets.

The discriminator performance from measurements on prototype chips is summarized below

Jitter:	350 pS 50fC into pre-amp
Prop delay:	13 nS 50fC into pre-amp
Time walk:	600 pS SPICE simulation (<1ns measured) over expected dynamic range of MDT signals.

2.6 Wilkenson Integrator

The function of the Wilkinson integrator is to measure the amplitude of the leading edge of the pulse for off-line time slew correction caused by the finite peaking time of the preamp/shaper plus the small time walk of the discriminator. It integrates a copy of the shaper output current into a holding capacitor in response to a gate generated by the Control Logic. The gate is short, of order one to two times the peaking time of the shaper to sample the leading edge of the pulse only. The charge held in the capacitor is then run down at a constant rate. Its return to baseline is sensed by a third discriminator (**Disc 3**) provided for this purpose only. The duration of the rundown is a measure of the leading edge amplitude and is used offline as a time slewing correction for leading edge resolution enhancement. It is anticipated that the Wilkinson mode pulse output will be in the range 20ns min, to 120ns max. i.e. 100ns maximum ADC range. This corresponds to 7 bit ADC dynamic range.

A block diagram is shown below in Figure 7.

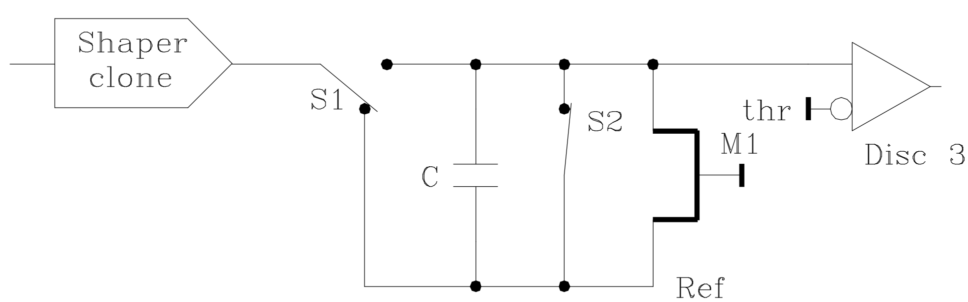


Figure 7

Gating for the switches comes from the control logic section (Fig 1). On receipt of a signal (firing of Disc 1, Fig 1) , a gate of approximately 20ns duration actuates both S1 and S2 thus pumping charge onto holding capacitor C and firing Disc 3 whose threshold is set just above the reference voltage (Ref). After the narrow gate, switch S1 returns to its initial state while S2 remains open until Disc 3 returns to its quiescent state, thus fully discharging the holding capacitor. Transistor M1 acts as a current source to discharge the holding capacitor during the run down. The trailing edge timing of Disc 3 is a measure of the charge in the leading edge of the pulse. The ADC output is the logical OR of the Gate and the Disc 3 output. It is in principle possible for very small signals to fail to fire Disc 3. In this case, the output pulse will be of a fixed duration equal to the gate width and will thus be recognizable as such. Timing of the sequence in the general case is shown below in Figure 8.

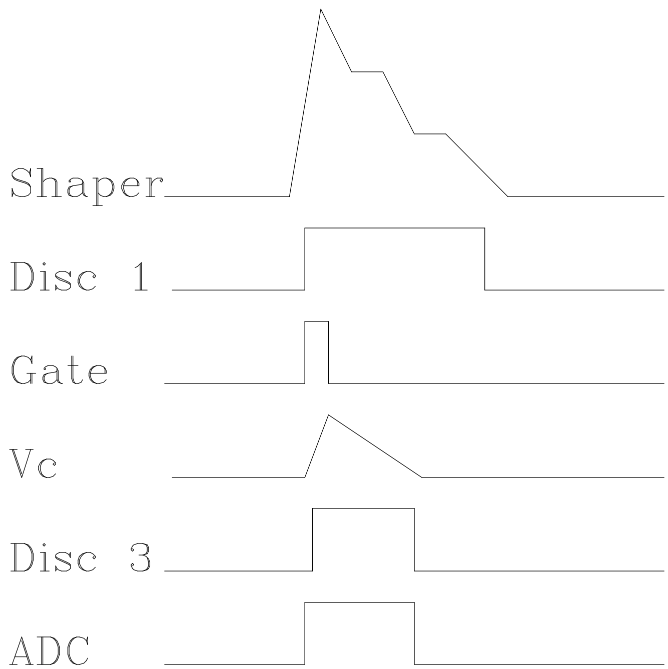


Figure 8

2.7 LVDS cells

There are two LVDS cells currently under study referred to as Type A and Type B as described below. Testing has already been done on the Type A cell, and upon completion of testing of both, one will be selected.

There are two common interpretations of the LVDS standard in use in experimental physics. The IEEE standard specifies that the common-mode voltage should be defined by the driver, and that the receiver should be high-impedance for common-mode signals. Alternatively, in some applications the common-mode voltage is set at the receiver. Our “Type B” cell is of the former type, while the “Type A” cell is of the latter type. The final ATLAS TDC will likely adhere to the IEEE standard, suggesting a “Type B” cell for the final design.

2.7.1 Type A

The schematic of the Type A cell is shown below in Figure 9.

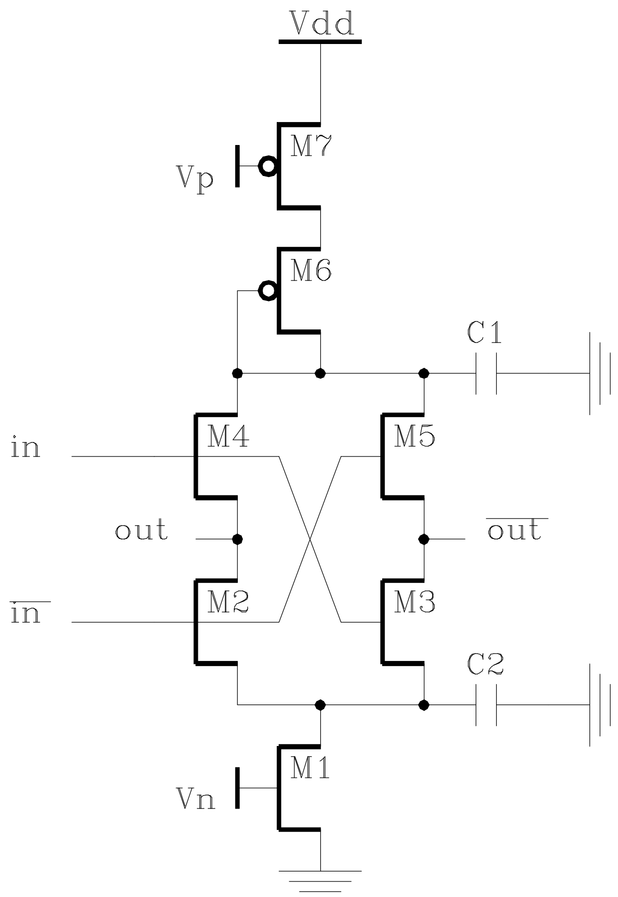


Figure 9

Current switching is accomplished by two pairs of nfets, M2/3 and M4/5. When M4 and M3 are 'on', current flows in the forward direction through the output (**out** to **out-bar**). When M2 and M5 are 'on', current flows in the opposite direction. The common-mode voltage is not determined by the driver and must be set externally by a termination network.

Diode connected transistor M6 provides a voltage offset to optimize the cell for use with a common-mode voltage in the 1.2V region, as recommended by the LVDS standard. Capacitors C1 and C2 reduce switching transients in power supply and ground rails.Two current mirrors (not shown) provide the reference current for the outputs. A single external reference current with a magnitude of 20% of the desired output current is required.

2.7.2 Type B

Schematic of the LVDS Type B[2] cell is shown in Figure 10 below.

[2] Suggested by O. Milgrome, LBL, private communication

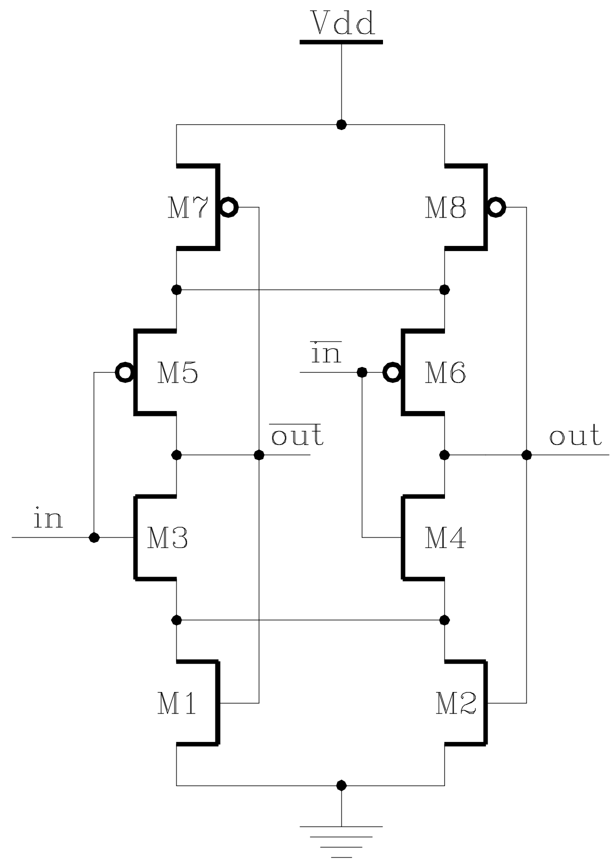


Figure 10

This cell utilizes common mode feedback and does not require external adjustments. Common mode feedback is provided by the M1/M2 and M7/M8 transistor pairs operating in their triode (resistive) region. Output common mode voltage is set at the driver and is fixed by relative transistor sizing.

2.8 I/O Pad Protection

I/O pads are divided into two categories; digital and analog i/o. Digital i/o pads will be protected from normal static discharges due to handling by pad protection circuits either obtained from standard cell libraries, or based on standard designs.

Analog input pads will be designed specifically for this purpose. They must provide esd protection, while at the same time, not degrade the performance of the preamplifiers which are connected to the MDTs. In particular, they must have low series resistance of order 10 ohms or less. While every attempt will be made to produce a robust design, **on-chip pad protection alone will not be relied upon to protect the MDT_ASD's inputs from high voltage discharges in the MDTs.** Traditional external protection circuits will be employed on the MDT "hedgehog" cards. These should protect the ASD's inputs from MDT discharges, anode wire breakage, and high voltage bypass capacitor breakdown.

3. Specifications

3.1 MDT Chamber Specs

It is anticipated that the MDTs may operate with a variety of gas mixtures and anode voltages. The front end chip (MDT-ASD) must be prepared to operate over this range by allowing for variable gain settings and variable tail cancellation time parameters. The following range of values is assumed.

a) Gas gain: **1e4 min, 8e4 max**

b) Tail cancellation time parameter **4 ns min, 15 ns max**

3.2 Analog linear range

The ASD has an inherently limited dynamic range which must therefore be optimally matched to the expected range of MDT signals. SPICE simulations tell us the relationship between pulses produced by primary electrons in the MDT and delta function pulses produced in calibration. For the values of gas gain listed above, the relationship is;

0.080 fc/pe @ 1e4 gas gain (LOW gas gain)
0.64 fc/pe @ 4e4 gas gain (HIGH gas gain)

where a primary electron is defined as a single electron avalanche occurring at the amplifier end of the MDT and thus suffers no attenuation along the resistive anode wire.

The ASD has a linear range of approximately one half of the power supply rail (3.3V) which we take, conservatively, to be 1.5 Volts. This linear range must be maintained through the shaping sections as nonlinearities in this section will produce pulse shape distortions and interfere with trailing edge measurements. The discriminator sections may be driven out of this range with no difficulty.

The choice we make is in mapping a fixed number of primary electrons in the MDT onto the linear range. The choice is made by measurements of muons and background photons which show that mapping the linear range onto the range 0 to 500 primary electrons is a reasonable choice.

N(linear range) = 500 primary electrons.

Given the gas gain and conversion to femtocoulombs, this sets the sensitivity of the analog sections as follows;

S = 1500mv/500pe = 3.0mv/pe

or

S = (3.0 mv/pe) / (0.08 fc/pe) = 37.5 mV/fc @ 1e4 gas gain

S = (3.0 mv/pe) / (0.64 fc/pe) = 4.69 mV/fc @ 8e4 gas gain

4. ASD-Lite

4.1 General

ASD-Lite is a 4 channel preamp/shaper/discriminator intended for prototype and production chamber testing. It is a dedicated device and has no digitally programmable modes or constants. Each channel consists of preamplifier, shaper, discriminator, and LVDS output driver. The discriminator output reflects the time over threshold of the shaped input signal. Of the four channels, an analog output of the shaped signal is provided in Channel 0 only for the purpose of MDT pulse shape studies. No Wilkenson mode is provided as off-line time walk correction, thus some chamber resolution degradation is expected as compared with use of the Wilkenson mode (MDT-ASD). The specifications are described in the following sections.

4.2 Specifications

4.2.1 MDT Operating point

The ASD-Lite will be optimized for MDT gas gain of 2e4

4.2.2 Preamp

Type : Unfolded cascode, input fet (nfet) W/L=2400u/0.9u
Input impedance : 100 Ω @ 1ma fet bias current
DC transimpedance : 20k Ω
Sensitivity : 1.1mv/fc
Power consumption : 3.3 mW per side (signal & dummy)
Bias adjustment : 1:2 current mirror adjustable from 150ua to 750ua external (300ua to 1.5ma input fet bias)
Offset adjustment: Depends on external components. Covers linear range of shaper output

4.2.3 Shaper

Type : 2 x pole/zero feedback topology
Time constant : Fixed positive ion tail cancellation time constant, t0=10ns
Pulse gain: tbd

4.2.4 Baseline Restoration

Type: Active blr loop
Time constant: 1 to 10 us by external bias adjustments

4.2.5 Calibration

Fixed on-chip calibration caps will be provided on each channel. There will be two strobe lines; one for **even** channels and one for **odd** channels.

4.2.6 Discriminator

Type: Unfolded cascode
Hysteresis: Adjustable via external bias

4.2.7 LVDS

Type: To be determined

4.2.8 Packaging

Type: To be determined (44 pin plcc or 44 pin soic)

5. MDT-ASD

5.1 General

The MDT-ASD will implement all the functionality shown in Figure 1, along with addressable register locations to hold values for adjustable parameters. These adjustable features are described in the following sections. At the time of this writing, the list of addressable locations and there functions should only be considered approximate. The will undoubtedly change as the specifications evolve and are listed for illustrative purposes only.

5.2 Process variations

The front end chip will be manufactured in the HP 0.5 micron n-well CMOS process. The front end chip performance is sensitive to several key process parameters and will have programmable features necessary to adjust for variations. A complete history of measurement data for the process is available from MOSIS and is used as the basis for estimating statistical variations. In addition, the vendor provides a “Wafer Acceptance Criteria” which we can use to extract worst case values. In all cases, a worst case analysis will be used. The two areas in which process variations are relevant are a) gain and b) tail cancellation shaping time.

Analog gain is dependent on three factors; capacitor values, resistor values, and transconductance. HP has implemented capacitors using its proprietary “linear capacitor” option using polysilicon over an n+ diffusion in a special “cap well” unique to its process. This structure has been used for some time in the 1.2 micron process and has been made available to the 0.5 micron process starting Feb. 1997. While wafer acceptance data do exist, we expect modifications in the published numbers as the process matures.

Resistors have been implemented using polysilicon with a special “silicide block” layer which increases its resistance from approximately 2 ohms per square, to approximately 100 ohms per square. This feature is available in the 0.5 micron process starting Feb. 97. Again, we expect measurement data on wafer acceptance to vary somewhat during 1997 and then settle down. For the moment, we use vendor “scrap limits” for min/max criteria. Measurements have shown that resistor tolerances within a given run are much tighter than this. It is anticipated that the entire run of MDT_ASDs will be produced in a single run and therefore will not incur wide chip to chip variations.

For the moment, we use the following tolerance for parameter variations taken from the HP specifications. Absolute values are HP proprietary and not reproduced here.

Parameter	tolerance
Polysilicon sheet resistance	30%
Linear cap capacitance/area	16%

Transconductance	6%

5.3 Component trims

5.3.1 Gain resistors.

There are four stages of amplification whose gain is determined by polysilicon resistors; one just following the preamp, two in the shaper, and a pre-discriminator gain stage. Alternatively, linerized fets may be used in their triode region as gain resistors. In either case, a trimming mechanism will be provided to trim the stage gains to predetermined values.

5.3.2 Tail cancellation capacitors.

The tail cancellation circuit consists of two stages of pole/zero filters. In each stage, the ratio of the pole time constant to zero time constant is set by design (resistor ratio and gain) while the pole location is set by capacitor values. To accommodate various shaping times, as well as capacitor process variation, the capacitance is programmed over a ~2.5:1 dynamic range. The nominal range is chosen to be 6ns to 16ns. Given a +/- 16% capacitor tolerance, this guarantees a range of t0 between 7ns and 13.5ns.

5.4 Modes of operation

*5.4.1 Time over threshold (**TOT** mode)*

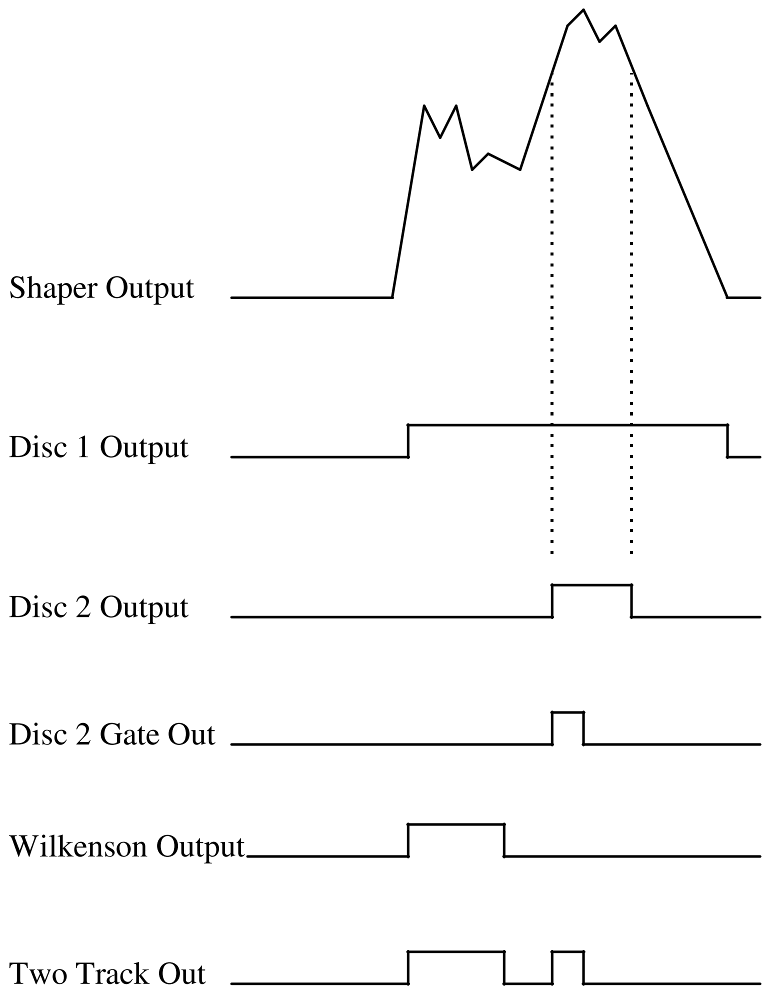
Output pulse is defined by the output of Disc 1 (Figure 1). Both leading edge threshold and hysteresis are programmable.

*5.4.2 Leading edge plus integrated charge (**Wilkinson** mode)*

Output pulse is true from the leading edge of Disc_1 to the trailing edge of Disc_3 and is thus their logical OR. Rundown time is programmable with an expected typical length of order 100ns (See Figure 8).

*5.4.3 Two track separation (**Two Track** mode)*

The output of the Wilkinson section is logically ORed with the output of the (~10ns) gate generator tied to Disc_2 (high level disc). Thus Disc_2 firings can be identified by their short duration. There is an inherent dead time (minimum two track separation) equal to the Wilkinson integrator output time.



Two Track Mode

5.4.4 Disc_2 gate

This is a test mode and presents the gated output of the high level discriminator to the output.

5.5 Programmable bit string

The addressable register space is arranged as a serial bit string whose ***preliminary*** assignments are listed below, followed by a discussion of their meaning and intended use. ***Note that this list is to be taken as an approximation and that both the number of bits and their precise assignments may, and probably will change.***

An attractive option is to have a RESET line to be used to power up the register bank in a reasonable default state. Thus only changes to this state need be programmed. This requires some additional real estate for Set/Reset flip-flops and associated routing. If the real estate usage is acceptable, this option will be provided.

			Bit location	
Name	**Bits**	**Function**	**Upper**	**Lower**
Boundary Scan TDC	8	JTAG outputs to TDC (LVDS)	141	133
Spare	2	Reserved	132	130
Enable mask	8	Enable analog channel	129	121
Cal inject mask	8	Enable cal inject channel	120	112
Cal inject bank	1	Enable differential cal inject	111	110
Cal inject caps	4	Cal-inject capacitor select	109	105
Bias current	4	Analog bias current	104	100
Gain resistor trim	4	Process and gas gain variation	99	95
Shaper resistor trim	3	Process variation	94	91
Shaping time	4	Shaper capacitor select	90	86
Wilkenson gate width	3	Wilkenson gate generator bias	85	82
Wilkenson ramp	4	Wilkenson ramp current select	81	77
Wilkenson cap	4	Wilkenson cap value select	76	72
LVDS bias current	4	LVDS bias current DAC	71	67
Disc_1 threshold	6	Discriminator threshold DAC	66	60
Disc_2 threshold	6	Discriminator threshold DAC	59	53
Disc_3 threshold	6	Discriminator threshold DAC	52	46
Disc_1 hysteresis	6	Discriminator hysteresis DAC	45	39
Disc_2 hysteresis	6	Discriminator hysteresis DAC	38	32
Disc_3 hysteresis	6	Discriminator hysteresis DAC	31	25
BLR	16	Baseline restoration	24	8
Control	5	Reserved	7	2
Mode control	2	Mode[00] : **TOT**	1	0
		Mode[01] : **Wilkenson**		
		Mode[10] : **Two Track**		
		Mode[11] : **Test : Disc_2 gate**		

5.5.1 Boundary Scan TDC

An eight bit mask which forces the assertion of an LVDS signal level on the MDT_ASD output pads to the TDC. This is for test purposes only. Its exact implementation is not yet determined.

5.5.2 Enable mask

Allows analog channels to be selectively enabled/disabled. Disabling removes power from that channel and can be used in the event of a noisy or otherwise unusable MDT channel.

5.5.3 Cal inject mask

Selection mask for calibration injection.

5.5.4 Cal inject caps, Cal inject bank

A four bit bank 16 calibration inject capacitors is placed at each preamplifier input. Cal Inject Caps selects from 1 to 16 cal of these for charge injection, while Cal Inject Bank selects either one or both preamps in the differential input structure.

Cal inject pulses correspond to fixed charge which must be chosen to span a useful range, which will naturally be a compromise for any given gas gain. The range is taken to correspond to

1 LSB = 15 (5) primary electrons at LOW (HIGH) gas gain.

Full Scale = 225 (75) primary electrons at LOW (HIGH) gas gain.

For a 1 Volt calibration strobe pulse, this corresponds to

1 LSB = 2.4 femtofarad
Full scale = 38.4 femtofarad

where the conversion factors in section 4 have been used.

By using Cal Inject Bank, the dynamic range is effectively doubled. Note, however, that since an MDT is connected to one preamp and not the other in each differential pair, the amount of charge injected into the preamp will be somewhat different for the two banks (~ 30% difference). Thus, Cal Inject Bank is not, strictly speaking, the MSB of the Cal Inject Caps word.

5.5.5 Bias current

DAC for setting the bias current level in the preamplifier and analog circuits.

I(preamp) = I(lsb) * (1 + N) N=0,...,15
1 LSB = 125 uA preamp bias current
Full scale = 2 ma
Nominal = 1 ma

5.5.6 Gain resistor trims

Trim load resistor after first differential amplifier for process variation and gas gain selection. Values to be determined

5.5.7 Shaper resistor trims

Trim load resistor in shaper stages for process variation to fixed value.

5.5.8 Shaping time

Selects capacitor values from a bank of 16 capacitors corresponding to nominal shaping time as follows;

$$T(0) = (9 + N)*2/3 \text{ ns}$$
$$T(min) = 6\text{ns}$$
$$T(max)= 16\text{ns}$$

5.5.9 Wilkinson gate width

Gate width adjustment is 4ns to 32ns as follows;

$$T(gate) = 4\text{ns} * (N + 1) \quad ; N = 0, .., 7$$

5.5.10 Wilkinson ramp

Four bit ramp current select. Value to be determined

5.5.11 Wilkinson cap

Determines value of holding capacitor for charge integrator/ Wilkinson rundown. May not be required in final version.

5.5.12 LVDS bias current.

Four bit setting for LVDS output cell. This will probably not be required in final version.

5.5.13 Disc_1 threshold (6 bit DAC)

Primary low level discriminator

1 LSB = 4 mv
Full Scale = 256 mv

5.5.14 Disc_2 threshold (6 bit DAC)

High level discriminator

1 LSB = 24 mv
Full Scale = 1.5V

5.5.15 Disc_3 threshold (6 bit DAC)

Wilkinson ADC discriminator

1 LSB = 4 mv
Full Scale = 256 mv

5.5.16 Disc 1 hysteresis (6 bit DAC)

1 LSB = 4 mv
Full Scale = 256 mv

5.5.17 Disc 2 hysteresis (6 bit DAC)

1 LSB = 4 mv
Full Scale = 256 mv

5.5.18 Disc 3 hysteresis (6 bit DAC)

1 LSB = 4 mv
Full Scale = 256 mv

5.5.19 Baseline Restoration

Reserved 12-16 bits

5.5.20 Mode control

MDT measurement mode.

5.6 Digital i/o protocol

The i/o protocol is JTAG standard.

5.7 Packaging

Final packaging is not yet decided. One possibility is a standard 68 pin plastic PLCC with the following tentative pin list.

Count	Pin No	Name	I/O type	Description
1	??	In0a	Analog In +	Charge Input
2	??	In0b	Analog In -	Dummy Input
3	??	In1a	Analog In +	
4	??	In1b	Analog In -	
5	??	In2a	Analog In +	
6	??	In2b	Analog In -	
7	??	In3a	Analog In +	
8	??	In3b	Analog In -	
9	??	In4a	Analog In +	
10	??	In4b	Analog In -	
11	??	In5a	Analog In +	
12	??	In5b	Analog In -	
13	??	In6a	Analog In +	
14	??	In6b	Analog In -	
15	??	In7a	Analog In +	
16	??	In7b	Analog In -	
17	??	Out0a	LVDS Out +	Output to TDC
18	??	Out0b	LVDS Out -	Output to TDC
19	??	Out1a	LVDS Out +	
20	??	Out1b	LVDS Out -	
21	??	Out2a	LVDS Out +	
22	??	Out2b	LVDS Out -	
23	??	Out3a	LVDS Out +	

24	??	Out3b	LVDS Out -	
25	??	Out4a	LVDS Out +	
26	??	Out4b	LVDS Out -	
27	??	Out5a	LVDS Out +	
28	??	Out5b	LVDS Out -	
29	??	Out6a	LVDS Out +	
30	??	Out6b	LVDS Out -	
31	??	Out7a	LVDS Out +	
32	??	Out7b	LVDS Out -	
33	??	TMS	TTL in	JTAG Test Mode Select
34	??	TCK	TTL in	JTAG Clock
35	??	TDI	TTL in	JTAG Data In
36	??	TDO	TTL out	JTAG Data Out
37		/TRST	TTL in	JTAG Reset
38	??	Vb1	Analog	Bias V 1 (bypass cap)
39	??	Vb2	Analog	Bias V 2 (bypass cap)
40	??	Vb3	Analog	Bias V 3 (bypass cap)
41	??	Vb4	Analog	Bias V 4 (bypass cap)
42	??	VREFout	Analog Out	Reference out
43	??	VREFin	Analog In	Reference In
44	??	CalP	Analog In	Calibration pulse +
45	??	CalN	Analog In	Calibration pulse -
46	??	AVdd	Power	Analog +3.3V
47	??	AVdd	Power	Analog +3.3V
48	??	AGND	Power	Analog Ground
49	??	AGND	Power	Analog Ground
50	??	DVdd	Power	Digital +3.3V
51	??	DVdd	Power	Digital +3.3V
52	??	DGND	Power	Digital Ground
53	??	DGND	Power	Digital Ground
54	??			
55	??			
56	??			
57	??			
58	??			
59	??			
60	??			
61	??			
62	??			
63	??			

64	??			
65	??			
66	??			
67	??			
68	??			