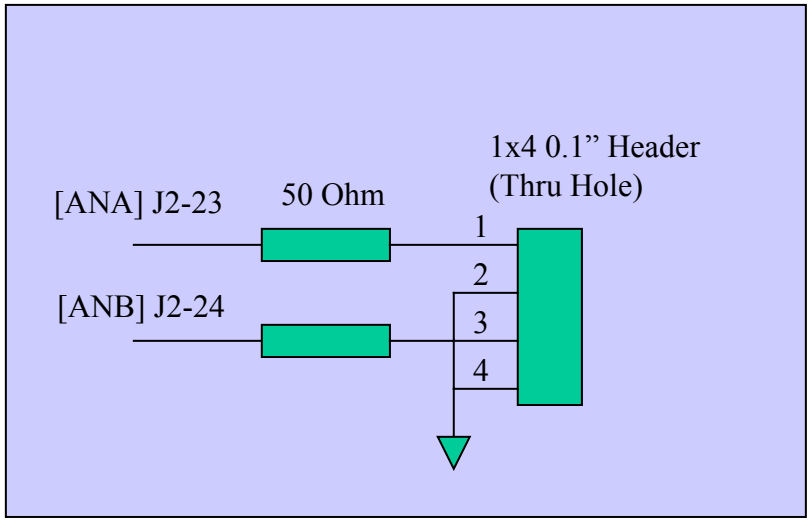
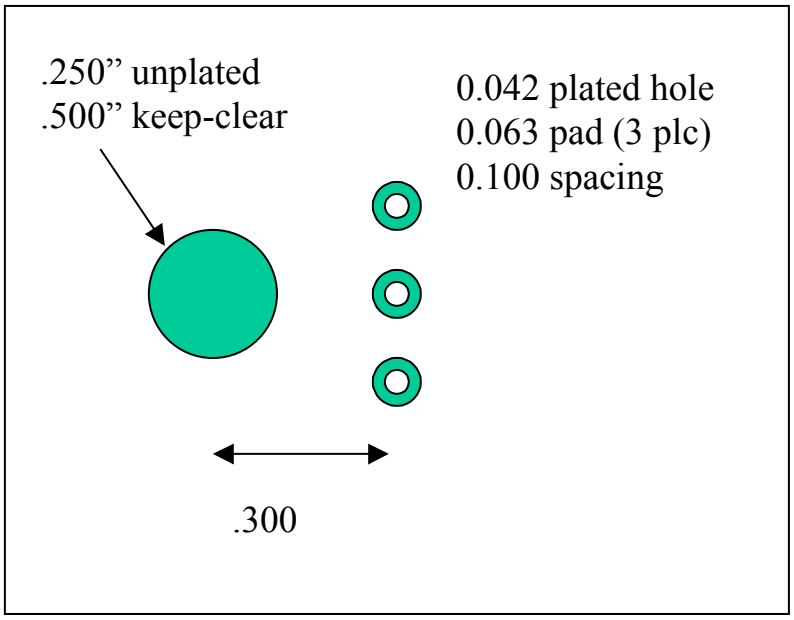
December 19, 2001
ATLAS Chip Tester Layout Notes

1. ANA, ANB signals (J2-23 and J2-24) connect as follows:

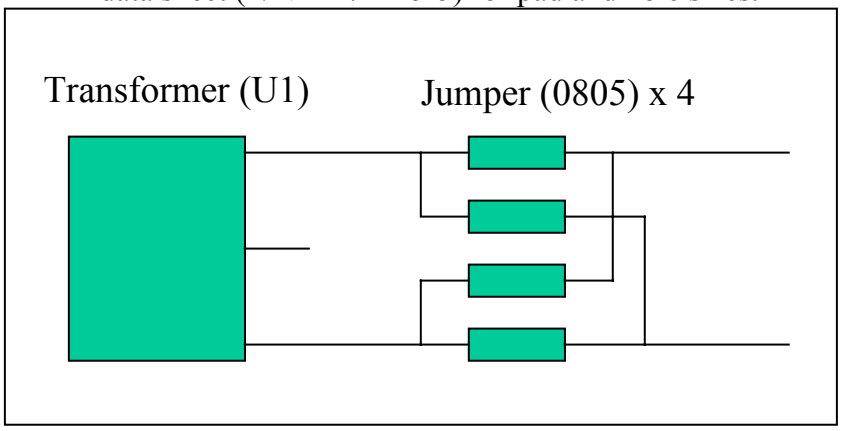


2. Add potentiometer as follows near U10A:

3. Component Footprint Issues:
   a. Fuses: use SMT fuse holder like Digi-Key P/N **F1224CT**. See data sheet "Fuse_holder_smt.pdf".
   b. All R/C except polarized caps are 0805 package
   c. Heatsink on voltage regulators suitable for 1A (3.5W) load – 2 square inches copper – layers 1,8 with thermal vias between. No soldermask on heatsink. Heatsink is ISOLATED electrically
   d. Mark LED polarity with "+" on Anode on silkcreen
   e. Mark capacitor polarity for all caps >= 1uF with + on silkscreen
   f. <u>Bypass Capacitors</u>:
      i. Digital Section – FPGAs
         4 ceramic (0805) caps at 4 corners + 1 tantalum (10uF) on top side for VCCINT *and* 4+1 caps on bottom side for VCCO.
      ii. Digital Section – other parts
         One ceramic (0805) cap *per power pin*.
      iii. Analog section – per schematic, on bottom side
   g. Switch SW1 footprint:



4. Carrier board gerber files to be supplied for mechanics
5. Connector pin assignments for 68-pin computer connector is attached. See AMP data sheet (P/N 2-174225-5) for pad and hole sizes.



6. Add “reversing circuit” to analog page (transformer output):
   LVDS terminators – 100 ohm between pairs as close as possible to FPGA.
   ASD Outputs (8 pairs) (OUTA0,OUTB0), (OUTA1,OUTB1)…
   ”BABAR” Outputs (16 pairs) (J1-3, J7-4), (J7-5, J7-6)…
7. 0.1” Clear area (no components) around FPGA body on top side
8. LVDS Pairs – route on layers 3,4 overlapped (stripline) 0.005” wide.
9. Connect FL_RT pin to new port “XINFLRT” which goes to any unused I/O on the FPGA.
10. 62.5 MHz clock (XRWCLK) – controlled impedance 0.005” wide on layer 3. Output from FPGA, under FIFO chips, terminate with two 120 ohm resistors per schematic.
11. General layout rules 0.005” traces, 0.005” spacing.
12. Copper pour on layers 1,8 should use 0.012” clearance and be connected to GND. (separate areas for analog and digital GND)

13. Layer Stack-Up:

No.	Use	Notes
1	Signal (top)	Copper Pour – AGND/DGND
2	AGND/DGND	
3	Signal	LVDS stripline
4	Signal	LVDS stripline
5	VDD_CORE (1.5V)	
6	Signal	62.5 MHz clock
7	VDD_FPGA (3.3V)	
8	Signal (bottom)	Copper Pour – AGND/DGND

Note: In general, route all signals longer than a few mm on layers 3, 4 and 6. (layers 1 and 8 should be mostly covered by the copper fill)