Production Testing of ATLAS MDT Front-End Electronics.

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Abstract

The production and testing of 360,000 channels of on-chamber electronics for the ATLAS Monitored Drift Tube system is described. The ASD front-end chips were tested on a custom-designed automatic tester, which performed full DC and dynamic tests on a packaged part in about 5 seconds per chip. The completed mezzanine boards will be tested and burned in at a rate of 150 per day in a custom test facility. Details of the tests are given along with some representative results.

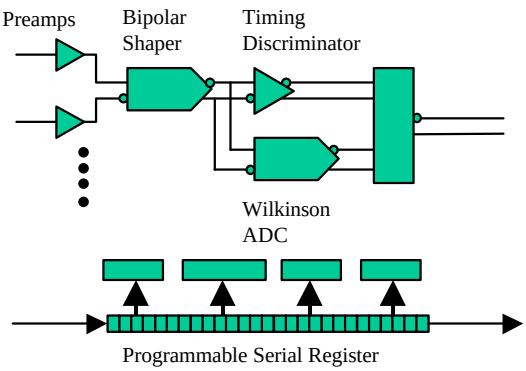
I. MDT Electronics Description

The ATLAS Monitored Drift Tube (MDT) system consists of 360,000 pressurized 3cm diameter aluminium drift tubes, filled with Ar-CO_2 at 3 atm. The tubes are glued in layers and assembled in super-layers of 3 or 4 layers. Two superlayers form a typical MDT "chamber". Each chamber is an electrically isolated entity, with DC power supplied, and only optical connections for signal I/O.

A. ASD Chip Design

Each tube is read out at one end by a full-custom CMOS Amplifier, Shaper, Discriminator (ASD) IC[1], and terminated at the characteristic impedance (360 Ω) at the far end where high voltage is also supplied. The ASD outputs are digitised by an ATLAS Muon TDC (AMT-3) IC[2]. A block diagram one ASD channel is shown in Figure 1:.

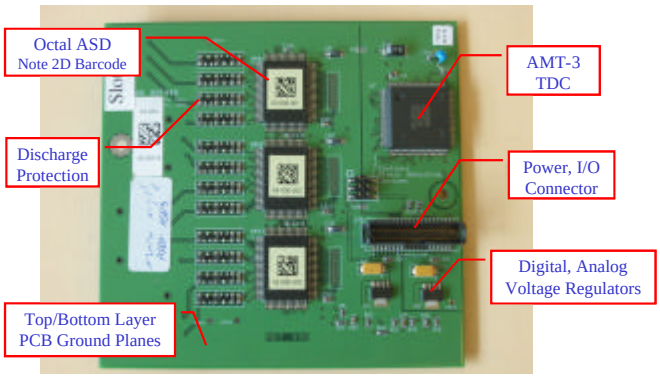
Figure 1: ASD Block Diagram



Each ASD channel begins with two identical transimpedance preamplifiers with a gain of about 1mV/fC. One preamplifier is connected to the drift tube, while the second is connected only to the package pin. Following the preamplifiers is a bipolar shaper implemented with three fully-differential amplifier stages and various passive feedback components. The fully-differential analog signal path provides immunity to pickup, power-supply noise and crosstalk.

Timing is measured using a leading-edge discriminator. A Wilkinson ADC measures charge in the leading edge of the pulse for offline time slew correction of the timing measurement. Programmable deadtime is provided. The ASD outputs are LVDS, with output pulse width proportional to input charge (other operating modes are selectable). Many parameters of ASD operation may be programmed using a simple serial interface.

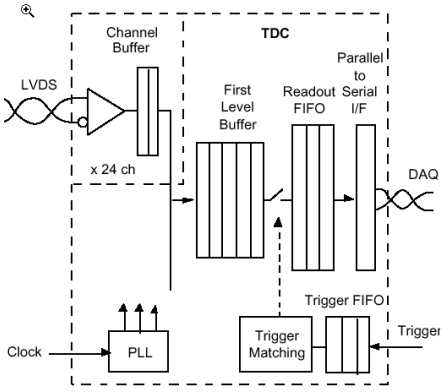
Figure 2: Photograph of Mezzanine PCB



B. AMT TDC and Mezzanine PCB

Three octal ASD chips are mounted on a mezzanine PCB along with one AMT-3 TDC (see Figure 2:) The TDC is implemented in 0.3µm CMOS Toshiba gate array, with a full-custom cell for the PLL fine time measurement. The least count of the AMT-3 is 0.78ns (12.5ns / 16) and the timing resolution is 280ps rms. The AMT-3 includes a 256-word level 1 buffer and trigger matching logic for operation in the LHC environment. Level 1 trigger inputs and TDC data outputs are implemented using a 40 Mbits/s serial LVDS interface.

Figure 3: Atlas Muon TDC Block Diagram

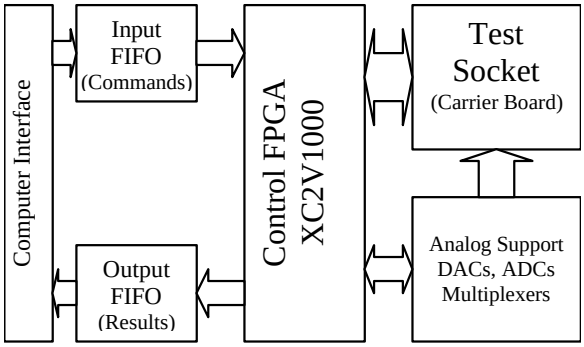


In addition, the mezzanine board contains two National Instruments LP3964 fixed 3.3V regulators, an LVDS buffer and a TMP036 temperature sensor.

II. ASD Chip Production

The ASD chips were fabricated in the HP/Agilent AMOS14 0.5µm CMOS process. A total of 5 production lots of 25 wafers each were ordered through MOSIS[3]. No wafer or die level testing was performed, based on others' reports of high yields in this process. A minimum of 15 good wafers were guaranteed per lot. We estimated that the 5 runs would yield a total of 67,500 good parts (45,000 are required for installation). In fact we achieved this yield of functional devices after packaging and testing only 4 lots. We are currently packaging and will test the remaining lot for additional spares.

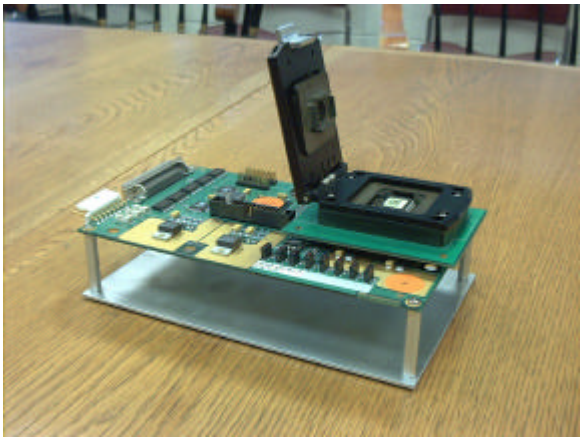
Figure 4: ASD Tester Block Diagram



A. ASD Tester Implementation

The packaged ASDs are tested on an automatic tester of our own design. A photograph of the tester and an overall block diagram are shown in Figure 4: and Figure 5:. The tester consists of a computer interface (National Instruments high-speed parallel I/O card), a main board and a mezzanine board. The main board contains two FIFO chips for input and output buffering of computer instructions and test results, a Xilinx XC2V1000 FPGA containing the control logic, and analog interface circuitry.

Figure 5: ASD Tester Photograph



Each ASD chip is serialized before testing with a 2D barcode sticker before loading in the tester. No chip loader robot is used; the test socket is loaded and unloaded manually by technicians. The overall average test rate was 2.5 devices/minute. A total of 72,000 devices were tested in 3 months on one test station.

The test socket was produced by AQL, Inc for us at a cost of about US$2,500. With occasional cleaning, the socket was 100% reliable after testing 72,000 devices. The key to its reliability is individually-sprung "pogo pin" contacts. Great care was taken in the layout of the supporting PCB to minimize inductance. Even so, only two well-separated channels of an ASD could be tested simultaneously, else the device would oscillate at low thresholds.

The ASD tester is controlled by a control program in Visual BASIC™ running on an attached PC. High-level instructions are written by the computer into the input FIFO. A command processor in the FPGA reads instructions one at a time, performs the specified tests, and writes the results to the output FIFO. A summary of important tester commands and returned results is shown in Table 1:.

Table 1: ASD Tester Commands

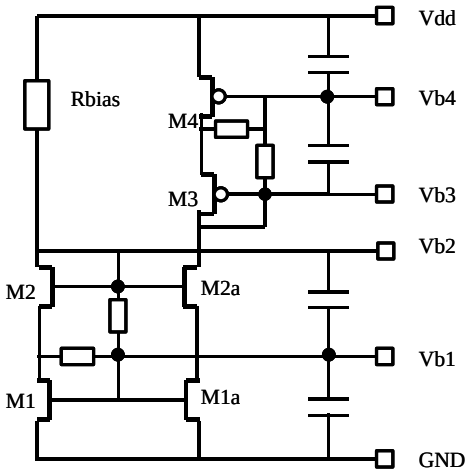
DC Tests		
Test Name	Input	Output
Bias Circuit Test	(none)	256 * 5 ADC values
LVDS Levels	(none)	16 ADC values
Preamp Input Levels	(none)	16 ADC values
Total DC Current	(none)	One ADC value
Dynamic Tests		
Noise Test	$V_{THRESHOLD}$	Time for 32 pulses
Wilkinson ADC (several tests)	ASD Mode ADC params	Measured Width
Deadtime	Channel No.	Measured Deadtime

Two test instructions will now be described in more detail.

B. Bias Generator Test

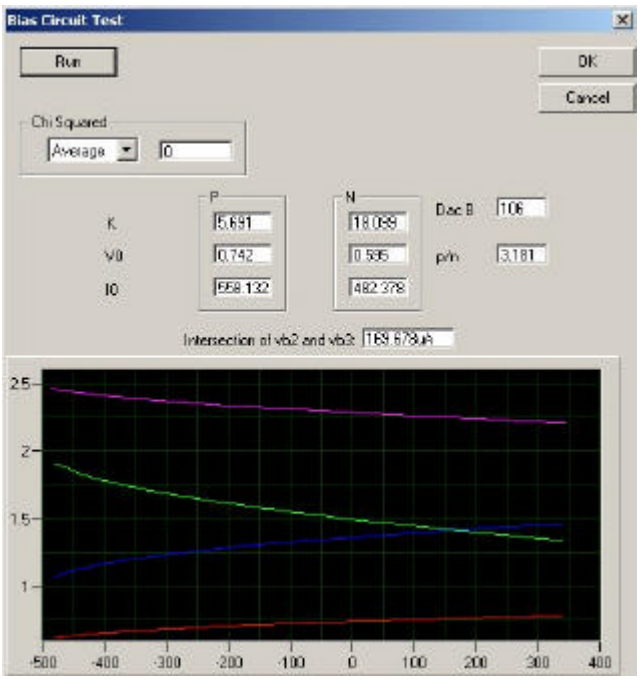
The ASD contains a bias voltage generator circuit shown in Figure 6: which produces four DC reference levels used throughout the chip. In normal operation the on-chip poly resistor Rbias provides the bias current. The bias generator test sweeps injects a variable current via Vb2 and measures the four bias voltages using an ADC.

Figure 6: ASD Bias Generator Schematic



A plot of the voltages Vb1..Vb4 is shown for a typical chip in Figure 7:. From this plot we can extract the basic transistor parameters V_{OFFSET} and $K'_{(N,P)}$. This is interesting but as it turns out not a useful predictor of the final "quality" of a tested chip. A go/no-go test on the bias generator consisted of testing Vb1..4 against upper/lower limits at the nominal (zero external current) bias point.

Figure 7: Bias Voltages vs. External Current



C. Threshold Sweep Test

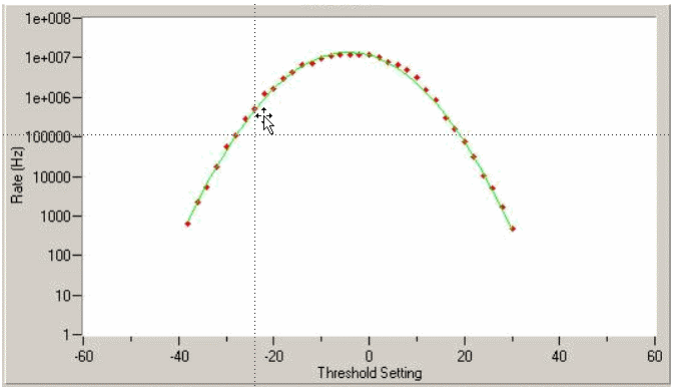
The most diagnostic test is the threshold sweep. This test takes advantage of the fact that the timing discriminator threshold is symmetrically programmable over a wide range about zero. In this test the threshold is swept through zero. At each threshold setting, the time required to accumulate 32 hits is measured, using a wide dynamic-range "floating point" counter. A typical results is shown in Figure 8:. Measuring a constant number of counts provides a constant error $\propto 1/\sqrt{N_{MAX}}$ for each point. The measured rates are fit to a Gaussian:

$$R(x) = \frac{2}{\sqrt{3}} \cdot f_{3db} \cdot e^{\frac{-(V_{offset}-x)^2}{2 \cdot s^2}}$$

The fit results (and their usefulness) are:

- Sigma (quite a sensitive measurement of various problems in the analog chain)
- Offset voltage (results in a correctable timing error; channels with negative offset are "hot", i.e. have high background hit rates)
- Peak hit rate at zero threshold

Figure 8: Threshold Sweep Plot

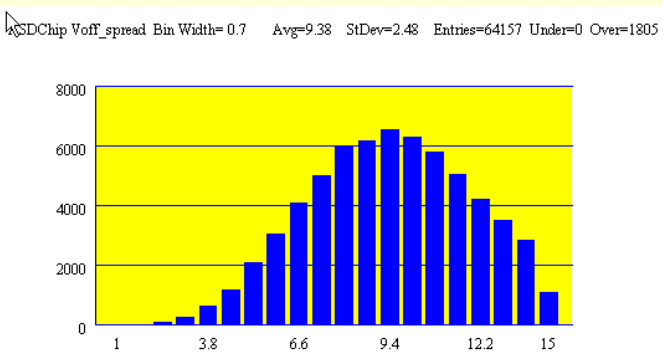


D. Summary of ASD Test results

The overall yield of functional ASDs is about 93%. There was one unexpected discovery which became apparent during testing—the spread of channel-to-channel offset voltages was larger than expected. Since there is one programmable threshold for an entire chip, the spread of offsets within a chip results in an error in setting the thresholds on some channels. A maximum spread of ±6mV was taken as a cut (compared to a typical threshold setting of 40mV (about 24 primary electrons). For worst-case channels with threshold 6mV below nominal, the noise hit rate increases from about 75Hz to about 3.7kHz.

With the ±6mV cut on offsets, the yield is reduced to 75%. This still allowed us to meet our production goal of 67,500 parts with 4 production lots (about 96 wafers). A histogram of the maximum peak-to-peak threshold offset for each chip is shown in Figure 9:.

Figure 9: Histogram of Threshold Offsets for 64K ASDs

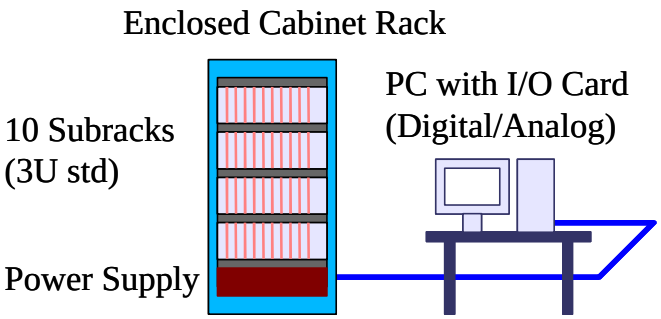


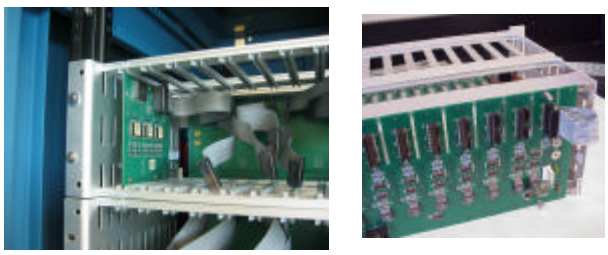
III. MEZZANINE BOARD PRODUCTION

A total of about 15,000 mezzanine boards must be installed in ATLAS. The boards are currently being assembled in Israel by two companies, and will be shipped to us in Boston for testing. We plan to perform a 24-hour elevated-temperature burn-in of each board, followed by a full functional test. Our expected burn-in/test rate is 150 boards per day.

Each mezzanine board is serialized before loading in the burn-in facility. The barcodes of each ASD on the board are read and recorded.

Figure 10: Mezzanine Board Burn-In Facility





A. *Mezzanine Board Burn-In Facility*

Each mezzanine board will be operated for 24 hours in a burn-in facility at an elevated temperature of about 60 deg. C. During burn-in, each board is supplied with power through a current-sensing and overcurrent-limit circuit. The current drawn on each of the two power supply inputs (analog and digital) along with the analog and digital voltage regulator outputs and temperature are logged continuously during burn-in. At the end of the 24-hour burn-in, the minimum, maximum, mean, and sigma of each measured quantity is recorded and compared against preset limits. If a failure is seen, the entire "strip chart" record of data may be examined or saved to study transient events (such as a tantalum capacitor self-destructing).

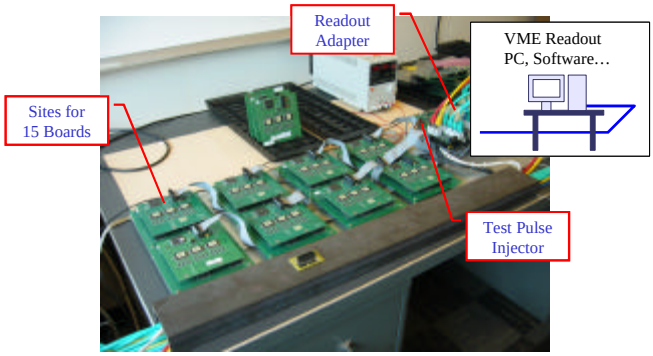
The burn-in facility (see Figure 10:) is constructed using industry-standard 3U sub-racks with a custom backplane. An adjacent PC with analog and digital I/O modules provides control and user interface software. A photo of a portion of the burn-in setup is shown in .

B. *Mezzanine Board Test Setup*

The mezzanine board test setup consists of a simple, passive carrier board, a test pulse injection board, and the "standard" ATLAS prototype DAQ setup. The carrier board contains passive termination components which simulate the MDT tube termination, and permit injection of test pulses on odd- and even-numbered channels. A companion PC provides control and user-interface software. A photo is shown in Figure 11:.

The principle behind the mezzanine board test is to detect both connectivity (solder) problems and components which fail during burn-in. A JTAG interface test is performed, followed by a pulse injection test where odd- and even-numbered channels are pulsed externally. This test is intended to detect crosstalk caused by short-circuits. Finally, a threshold sweep similar to that described in Section C above is performed. This test not only provides a thorough go/no-go test of the entire signal path (including the AMT-3 TDC), but is also sufficiently sensitive to detect the noise contributed by the external termination resistor on the carrier board. This ensures the connectivity of the input chain (connector, ESD protection circuit) on the mezzanine PCB.

Figure 11: Mezzanine Board Test Setup



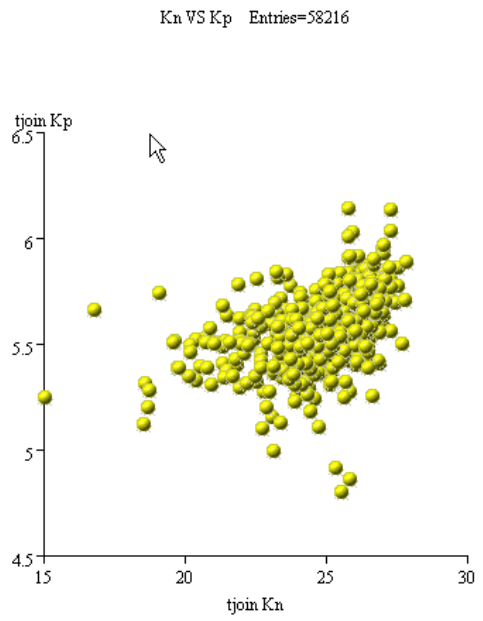
IV. DATABASE

Test results from ASD and mezzanine board tests are stored in a comprehensive database implemented using Microsoft Access™. A web interface provides extensive query and plotting facilities. It is intended to maintain the database and provide remote access throughout the operation

of ATLAS, so that any systematic effects which may be traceable to tested parameters may be investigated.

Samples plots extracted via the web interface may be seen in Figure 9: and Figure 12:.

Figure 12: Scatterplot of K_P vs K_P from ASD Database



An interesting bonus is the ability to identify mezzanine boards and (to a certain extent) ASD chips by their "signature" of threshold offsets as stored in the database. By performing a *Monte Carlo* analysis based on stored offset data, it can be shown that any individual mezzanine board can be identified with 99.999% accuracy by an *in situ* threshold sweep measurement after installation.

V. Summary

We have tested 72,000 ASD chips in 3 months using a full-function tester of custom design. A facility has been constructed to burn-in and test 15,000 assembled PC boards at a rate of 150 boards per day. This provides an example of how LHC-scale electronics can be produced and tested using resources available at well-equipped university electronics facilities.

VI. References

1. "CMOS front-end for the MDT sub-detector in the ATLAS Muon Spectrometer, development and performance", C. Posch, LECC2001 Conference, Stockholm, Sweden.
2. "Developments of a New TDC LSI and a VME Module", Y. Arai, Contribution paper to the 2001 IEEE Nuclear Science Symposium, San Diego, Nov. 3-10, 2001
3. See `http://www.mosis.org`