Preliminary Design Review

ATLAS MDT Electronics

Abstract

The PDR of the MDT electronics has been held at CERN on February 22nd 2001. This report gives a few recommendations.

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Distribution: EB Members, MDT Members, all participants mentioned in the report.

PURPOSE OF THIS REVIEW

The purpose of the Preliminary Design Review was to review:

- the requirements and specifications;
- the proposed architecture;
- the prototypes performances;
- the remaining developments;
- the application of ATLAS rules such as the radiation hardness assurance, the grounding scheme,...

MEMBERS OF THE REVIEW COMMITTEE

Review Committee

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SCOPE OF THE REVIEW

The Preliminary Design Review has addressed the following points:

- Front-end ASICs (ASD and TDC);
- Front-end boards;
- Read-out architecture (including the read-out driver);
- Radiation tolerance;
- Control.

AGENDA

1) System architecture target performance	J. Oliver
2) HV Hedgehog boards HV modularity, HV tests	A. Lanza
3) Signal Hedgehog Boards different chamber geometries	E. Hazen
4) Specifications, design and performance of the Octal ASD	C. Posch

5) Design, specs, performances of the AMT TDC	Y. Arai
6) Design of mezzanine boards electronics	E. Hazen
7) The Chamber Service Module (CSM)	J. Chapman
8) Meas'd system performance	J. Guimaraes
9) The MDT ROD (MROD)	A. Konig
10) Radiation tolerance issues	R. Richter
11) Sharing of responsibilities, costing, time schedule	G. Brandenburg
12) Reviewers Session and Close out.	

AVAILABLE DOCUMENTATION

The basic reference document is the MDT TDR, Chapter 5.4. Additional and more detailed documentation and information is available under the following address:

http://wwwatlas.mppmu.mpg.de/atlas_mdt/PDR/pdr_mdt_elx_02_2001.html

REVIEW OUTCOME AND RECOMMENDATIONS

1.1 EXECUTIVE SUMMARY

The committee was very impressed by the large amount of high quality work that has been done. Documentation was quite complete and easily accessible.

The four following points need to be tackled very quickly:

1. A new estimate of the single channel occupancy, front-end electronics dead-time, track reconstruction efficiency and read-out bandwidth requirement should be made with the new background estimation (AV5).
2. The estimated power dissipation of the front-end electronics is higher by a factor almost two than the expected one, because of later changes in the readout strategy, additional interfacing electronics and the necessity of voltage regulation at the level of the mezzanine boards. The Technical Co-ordination should be contacted as soon as possible in order to know whether this is acceptable or if a cooling system is needed.
3. A reliability analysis as well as the identification of single points failure should be done.
4. The amount of electronics in the cavern is large and there are some complex chips (e.g. FPGA's in the CSM). The components pre-qualification tests have to be done as soon as possible according to the "ATLAS Policy on Radiation Tolerant Electronics revision 2". In particular the technologies chosen for the front-end chips have not yet been fully qualified.

1.2 ASD CHIP

1.2.1 ASD shaping

With a dead time of 0.5us, the choice of a bipolar shaping with a short area balanced time seems well appropriate and more robust and simple than a baseline restorer. However, due to the presence of multiple after pulses, there is a potential risk that baseline shift caused by the bipolar shape extends well beyond 500 ns and impact the next hit specially for high background levels as recently expected. So, in the opinion of reviewers a shorter area balance time, i.e 100 to 200 ns would have been more robust in high background conditions. This shorter negative under shoot would not impact noise that is dominated by the resistor termination and would just shift more after pulses that are

anyway discarded. The reviewers understand that such a design change may not be compatible with the production schedule and they acknowledge the fact that the proposed scheme works fine with an average rate up to 400 kHz. However it is recommended to simulate with the new background estimation.

ASD has also not yet been tested with 6m long tubes. This should be done as the tube length may influence the ASD behaviour.

1.2.2 ASD Power dissipation

The power budget of the ASD, 35 mW/channel is already the total power budget allocated for the one channel of MDT front-end electronics in the TDR. However it is the result of an improved design (last version was consuming 48 mW/channel). It seems there could be room for decreasing power in amplifier stages by decreasing bias current. Lower bias currents will increase the series noise of the input transistor without real impact on the total noise. Simulations of amplifier performance versus power would be useful to evaluate possible power saving. Lower output current in the LVDS stage (1mA for low output current LVDS instead of 3 mA) could also substantially save power but would require of change of the TDC LVDS receiver.

If there is no way to reduce the power consumption without either major changes in the design(s) or performance degradation, a cooling system may be necessary.

1.2.3 ASD Single Event latch-up (SEL) issue

No study was presented for SEL risk assessment and no anti latch-up protection is currently implemented in the mezzanine cards. In the opinion of reviewers, some action should be done to evaluate ASD SEL risk and protect mezzanine cards against latch-up failure if ASD turns out to be latch-up susceptible. The evaluation of single event effects (SEE) risk should follow the ATLAS recommendation. If latch-up protection is necessary, simple current limiting circuit and over-current detection should at least be implemented to avoid any catastrophic failure of the mezzanine card. Latch-up protection can also be obtained by using dedicated anti-latch-up ASICs. The over-current monitoring would allow to perform the de-latching operation by switching off for a short time the concerned LV power supply.

1.3 AMT TDC CHIP

The AMT chip works accordingly to specification. The chosen technology has been tested successfully against total dose effects. SEE tests still need to be done, in particular SEL tests.

Simulation with the new background rate estimate must be done to check that the size of the internal buffers is sufficiently large.

According to the presented schedule, the production may start before a large system test is performed; this may be a bit early there may be the risk of producing a chip with undetected problems.

1.4 HEDGEDOGS

The HV hedgedogs are in very good shape and all the components to be used have been identified and tested at the exception of the protection resistors. The access to these boards is not easy and hence the reviewers recommend an estimation of the reliability to be done. Some burn-in procedure is foreseen during the production process. In addition there should be an easy way to identify the faulty boards.

The signals on the hedgedogs are unshielded in order to avoid high capacitance which would introduce variations in peaking as a function of the trace lengths. The resulting long unshielded wires

could lead to pick-up problem. In due course a test including the surrounding detectors (e.g. RPC) and the faraday shield should be done in order to verify there is not too much pick-up noise.

1.5 MEZZANINES

In addition to the ASD and AMT chips, the mezzanine boards house LVDS drivers and receivers. These chips must also be tested against radiation. The grounding and shielding concept has been successfully tested.

The reviewers recommend that the ATLAS TC be contacted as soon as possible to address the issue of power dissipation. If the current power consumption is too high and a cooling system is to be implemented, the design of this board is likely to be strongly affected.

1.6 CHAMBER SERVICE MODULE (CSM)

The proposed implementation based on the use of large FPGAs (Xilinks Virtex) seems a bit complicated to the review committee who would prefer a scheme where the full complexity is put in the MROD. Although SEU issue in Xilinks Virtex FPGA should be cross checked with results obtained by the RPC team, only data coming from ESA (European Space Agency) are known to the review committee. According to these data, only QPRO Virtex FPGA are qualified to radiation (TID = 100Krad, SEE tested, latch-up immune). Standard Virtex planned to be used in CSM boards are not qualified against radiation. Latch-up immunity should be clarified and SEE risks evaluated. Existing data on QPRO Virtex (XQVR300) show that there LET threshold is 3 $MeV.mg^{-1}.cm^{-2}$ in configuration cells with a cross section in the range 10-2 to 10-4 cm2/device. To circumvent SEE problems, triple input /output redundant registers, for clock data and reset, with triple voting have been proposed (for Space applications). It would be worthwhile to also consider this solution for CSM design. Reliability and robustness of CSM is particularly important because it is a single point failure in the MDT readout chain.

The path for the control and configuration is not completely clear. Except if redundancy is necessary a choice should be made between the DCS (CANbus and ELMB) and a separate JTAG path.

1.7 MROD

The committee does not fully understand why there is a need for so many high performance digital signal processors (SHARC's) and what is the level of data processing to be done.

1.8 RADIATION HARDNESS

The main ATLAS rules for prototyping and production are defined in the ATLAS Policy on Radiation Tolerant Electronics revision 2 available on the ATLAS electronics WEB site.

To avoid unexpected problems with radiation at the end of the prototype development, it is recommended to perform without delay the radiation tests required for pre-selecting generic components.

It was noted during the presentation that the radiation levels used were not up to date. The last computed numbers are given in Appendix I. The numbers to be taken into account are the ones obtained for the worst location (EIS/EIL chambers) and hence the tests must be done with this target dose and fluence. However it is understood that it may be possible to have a special treatment of the hottest locations in case of difficulties to characterise the electronics. Such a decision will have to be studied in due course, i.e. when the radiation tests have been finished and all the access and maintenance scenari are understood.

With the aim of improving the co-ordination of radiation hardness assurance works a new organisation, summarised in Appendix II, has been agreed upon. Most of the pre-selection tests should be completed before the end of 2001. A list of actions for 2001 is summarised in Appendix III. Most of the tests should be done in the second half of the year.

An interactive radiation test agenda is available on the web. (http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm#Radiation Facilities). MDT collaboration is kindly invited to put the dates decided for its radiation test campaigns in this agenda.

1.9 SHEDULE AND RESSOURCES

Production schedule is relatively aggressive. ASD will be in the final prototype phase in the next coming months, and there is no schedule after MPW submission to do an engineering run (pre-production) before launching the volume production. This seems a bit risky to the review committee.

It is also reminded that the production cannot start before all the radiation tests have been done and analysed.

Although this is not strictly in the field of competance of this review, the problem of who actually designs the final CSM version and who pays it seems rather serious. The planning looks problematic as a "final" CSM must be ready to qualify all the electronics to be mounted on the chamber.

A large system test should be done before launching the full production of ASICs and boards.

1.10 POWER SUPPLIES

Nothing was presented on this subject.

Appendix I : Radiation levels and radiation tolerance criteria

I.1. SIMULATED RADIATION LEVELS (SRL) FOR MDT ELECTRONICS LOCATIONS:

	BIS/BIL	BMS/BML	BOS/BOL	**EIS/EIL**	EMS/EML	EOS/EOL
SRL_{tid} (Krad)	0.47	0.28	0.13	***0.64***	0.62	0.33
SRL_{niel} (1 MeV eq. n/cm^2)	0.3×10^{11}	0.3×10^{11}	0.24×10^{11}	***2.9×10^{11}***	0.34×10^{11}	0.17×10^{11}
SRL_{see} (>20 MeV h/cm^2)	0.54×10^{10}	0.57×10^{10}	0.46×10^{10}	***4.8×10^{10}***	0.9×10^{10}	0.3×10^{10}

(see http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadConstraint/Radiation_Tables_181100.pdf). SRL are computed for 10 years of operation. The basis for computing RTCs is: column EIS/EIL.

I.2. TOTAL IONIZING DOSE RADIATION TOLERANCE CRITERIA FOR MDT ELECTRONICS:

Device type	SF_{sim}	SF_{ldr}*	SF_{lot}	SF product	RTC_{tid} (Krad) **
Standard COTS (unknown batch)	3.5	5.0	4	70	45
Standard COTS (known batch)	3.5	5.0	1-2	18-35	11-22
Rad-hard ASICs (known batch)	3.5	1.5	1	5.3	3.5

(*) TID tests made without post-irradiation ageing; (**) $RTC_{tid} = SRL_{tid}$ (EIS/EIL) x SF product

I.3. NON IONIZING ENERGY LOSS RADIATION TOLERANCE CRITERIA FOR MDT ELECTRONICS:

Device type	SF_{sim}	SF_{ldr}	SF_{lot}	SF product	RTC_{niel} *** (1 MeV eq n/cm2)
COTS (unknown batch)	5	1	4	20	5.8×10^{12}
COTS (known batch)	5	1	1-2	5-10	$1.5\text{-}3.0 \times 10^{12}$
Rad-hard ASICs (known batch)	5	1	1	5	1.5×10^{12}

(***) $RTC_{niel} = SRL_{niel}$ (EIS/EIL) x SF product

I.4. SINGLE EVENT EFFECTS RADIATION TOLERANCE CRITERIA FOR MDT ELECTRONICS:

There are three kind of SEE:

- Soft SEE (errors, upsets in memories);
- Hard SEE (bit stuck in a memory);
- Destructive SEE (latch-up, burnout, gate rupture):

RTC_{see} are the maximum rates of soft, hard and destructive SEE acceptable for MDT electronics. These maximum SEE rates must be determined by MDT collaboration according to system considerations. *They cannot be deduced from SRL_{see}.*

For safety reasons (risks of fire), components that are sensitive to destructive SEEs are not allowed in ATLAS electronics, unless a proven robust architectural solution protects the system against SEE induced fire.

Standard ATLAS SEE tests allow one to estimate SEE rates in a given ATLAS location.

The acceptance criterion for pre-selection SEE tests and for qualification SEE tests are:

- Foreseen rate of soft SEE < $RTC_{soft\cdot see}$
- Foreseen rate of hard SEE < $RTC_{hard\cdot see}$
- Foreseen rate of destructive SEE = 0 or < $RTC_{dest\cdot see}$ plus protection against fire risks.

For more details on SEE tests, see §.2.2 p.14 in ATLAS Policy on Radiation Tolerant Electronics rev. 2.

Appendix II : New organisation of RHA[1] in MDT collaboration

Organisation:

(a) For each MDT board, RHA is supervised by 1 person whose main tasks are:

- Write the list and number of all the components to be mounted on the board [form (2)];
- Summarise information on each type of component to be used on the board [forms (3)&(4)];
- Define and write test set-ups for every radiation test to be done; send it to (b);
- Organise and execute (or supervise) radiation tests for each component of the board;
- For each tested component, analyse results with (b) and (c) and write radiation test reports [form (5)]

(b) For the whole MDT electronics, RHA is supervised by 1 person[2] whose main tasks are:

- Designate the persons responsible for RHA for each MDT board and fill form (1);
- Plan radiation test campaigns to be done in 2001, for every board;
- Supervise radiation hardness assurance for the whole MDT electronics;
- Gather new or updated forms (2) to (5) completed by (a) and send them to (c);
- Help (a) to prepare radiation tests and to analyse results;
- Decides with (c) and with the ATLAS Electronics co-ordinator to accept or to reject pre-selection of generic components and qualification of batches;
- Write periodical global status reports on RHA for the whole MDT electronics;
- Build and maintain a web page on MDT Radiation Hardness Assurance (containing forms (1) to (5), plus periodical global status reports on RHA for MDT electronics, etc.).

(c) For the whole ATLAS experiment, RHA is supervised by 1 person[3] whose main tasks are:

- Define and supervise radiation hardness assurance for the whole experiment;
- Advise ATLAS sub-systems for the selection of radiation tolerant electronics;
- Help (a) and (b) to prepare radiation tests and to analyse results;
- Organise access to radiation facilities for every ATLAS sub-system;
- Decides with the (b) and with the ATLAS Electronics co-ordinator to accept or to reject pre-selection of generic components and qualification of batches;
- Write periodical global status reports on RHA for the whole ATLAS electronics;
- Co-ordinate ATLAS RHAWG, build and maintain ATLAS Radiation Hard Electronics web page, build and maintain ATLAS Radiation Test Agenda, etc.

Reporting line:

- (a) reports periodically to (b) and (c) and to the MDT management;
- (b) reports periodically to (c) and to the MDT management;
- (c) reports periodically to ATLAS Technical Co-ordination[4].

Standard forms:

(1) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/ListOfBoards.doc
(2) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/QuantityPerBoard.doc
(3) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/PreselectionTables.doc
(4) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/QualificationTables.doc

[1] RHA : “Radiation Hardness Assurance”
[2] R. Richter
[3] M. Dentan
[4] P.Farthouat and M. Nessi

(5) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm#Standard Test Methods

Appendix III : Summary of RHA actions to be done by MDT in 2001

Action	Date	Who?
Complete the list of the persons responsible of RHA for each MDT board (form available at the address (1) below); transmit this list to ATLAS/TC/ELEC/RHA.	Before end-April	(b)
Complete the table "quantity per board" given in (2). Transmit it to ATLAS/TC/ELEC/RHA.	Before end -April	(a) and (b)
Complete the table "summary of pre-selection tests" given in (3), even if tests are not already completed, and transmit it to ATLAS/TC/ELEC/RHA.	Before end -April	(b)
Complete the table "summary of qualification tests" given in (4) and transmit it to ATLAS/TC/ELEC/RHA.	Every 3 months during qualifications	(b)
For every component already tested, write radiation test report using new standard ATLAS forms available on the web (5), and transmit them to ATLAS/TC/ELEC/RHA.	Before end –April (if results available)	(a)
For every component not yet tested or partially tested, complete the pre-selection tests.	Before end-2001	(a)
For every radiation test to be done, write a description of the test set-up to be used and submit it to ATLAS/TC/ELEC/RHA.	2 weeks before the radiation test	(a)
For every component newly tested, write radiation test report using new standard ATLAS forms available on the web (5), and transmit them to ATLAS/TC/ELEC/RHA.	1 week after the end of the radiation test	(a)
When radiation test results complies with the acceptance criteria defined in ATLAS Policy on Radiation Tolerant Electronics: ⇨ notify[5] ATLAS/TC/ELEC/RHA and go ahead.	2 weeks after the end of the radiation test	(b)
When radiation test results don't comply with the acceptance criteria defined in ATLAS Policy on Radiation Tolerant Electronics: ⇨ Analyse test results with ATLAS/TC/ELEC/RHA in order to decide on future actions.	2 weeks after the end of the radiation test	(a), (b) and (c)

(1) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/ListOfBoards.doc
(2) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/QuantityPerBoard.doc
(3) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/PreselectionTables.doc
(4) http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/RadTestReport/QualificationTables.doc
(6) Section 4 in http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm

(a) Person responsible for radiation hardness assurance of the board containing the tested device(s);
(b) Person responsible for radiation hardness assurance of the whole MDT system (R. Richter);
(c) Person responsible for radiation hardness of the whole ATLAS experiment (M.Dentan).

[5] Send the radiation test reports together with the notification to ATLAS/TC/ELEC/RHA.

Appendix IV : Access to radiation facilities organized by ATLAS/TC

ATLAS/TC/ELEC/RHA organises access to the radiation facilities below with negotiated prices for ATLAS systems in 2001. MDT is invited to book for radiation campaigns as soon as possible.

1. SEE TESTS AT CRC (UCL, LOUVAIN-LA-NEUVE, BELGIUM):

Beam: 20-60 MeV protons; diameter: 9 cm; maximum flux: 5E8 cm^{-2} s^{-1}.
Devices must be biased, operated and measured on line during tests;
Dates: 20 June, 20 August and 15 Decembre 2001 (provisional dates);
Access to the CRC facility organised by F. Faccio[6].
Booking: 3-4 weeks in advance, or more (recommended).
Prices negotiated by CERN: 200 Euro per hour.

2. TID TESTS AT PAGURE (CIS-BIO-INTERNATIONAL, SACLAY, FRANCE):

Gamma photons (60Co): 1,17 MeV and 1,33 MeV;
Maximum dose rate: 1,6 Mrad per hour;
Devices must be biased during tests. On-line or off-line measurements (free choice);
Dates: 29 June, 28 Septembre and 29 Novembre 2001 (provisional dates);
Access to the Pagure facility organised by M. Dentan;
Booking: 3-4 weeks in advance, or more (recommended);
Prices negotiated by ATLAS TC/ELEC/RHA: around 900 Euro per day for 6 sectors of 60 degres (shared price if several users; reduced price if shorter irradiation period of if less than 6 sectors are used).

3. NIEL TESTS AT PROSPERO (CEA, VALDUC, FRANCE):

1 MeV equivalent neutrons (peak at 700 keV);
Accurate calibration, very low residual TID;
Devices can be irradiated with or without biasing. Measurements can be made on-line (immediate results) or off-line (after 1 month deactivation);
Dates: 5 July, 2 Octobre and 6 Decembre 2001 (provisional dates);
Access to the Prospero facility organised by M. Dentan;
Booking: 2-3 weeks in advance (recommended);
Prices negotiated by ATLAS TC/ELEC/RHA: 2280 Euro / half day; 4560 Euro / full day (shared prices if several users).

4. ORGANISATION FOR THE PAYMENT OF RADIATION TESTS MADE AT PAGURE AND AT PROSPERO:

ATLAS TC/ELEC/RHA negotiates prices with radiation facilities, organise radiation tests and pays the radiation facilities for these tests;
ATLAS sub-systems which participate in irradiation campaigns organised by ATLAS TC/ELEC/RHA reimburse ATLAS TC/ELEC/RHA according to their use of the radiation facilities.

5. PAYMENT OF RADIATION TESTS MADE AT CRC (UCL):

Payment must be made directly to the radiation facility.

[6] CERN/EP; Federico.Faccio@cern.ch