Simulated Radiation Levels and Current Test Status for ATLAS MDT Front-End Electronics

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Introduction

The ATLAS policy on radiation-tolerant electronics makes a rather drastic simplification: it is assumed that the worst-case simulated radiation level (SRL) applies to all instances of a particular electronic component. This is of course not the case. In many cases the cost of making all instances of a component sufficiently rad-tolerant to survive in the worst-case location is impractical for cost or other reasons. This note presents a more detailed analysis of the radiation levels for various locations in the ATLAS MDT system.

Method

The location in (R,Z) was determined for each MDT Mezzanine board in the MDT system from the MDT system layout parameter book version 'Q'. At each mezzanine board location, the SRL was extracted from the June 2001 baseline radiation level table. Manual comparison with the latest available plots (from June 2002) showed little difference in SRL_{TID} or SRL_{NIEL} between the two simulation runs.

The MDT layout parameter book ¹ gives the locations of all 1,172 MDT chambers in ATLAS. Each chamber type (BIL, BIS etc) has its own sheet in the spreadsheet. The individual sheets were saved to CSV files for convenient processing. In addition, the radiation tables from June 2001² were downloaded and saved as CSV files. A C++ program was used to read the parameter book data, and for each chamber the R, Z coordinates of the mezzanine boards were calculated. The results were loaded into a spreadsheet program, sorted in decreasing order of SRL, and plotted.

Results and Implications

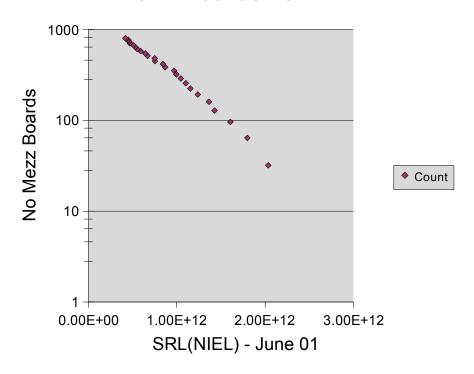
The results are plotted below. In Plot 1, the number of mezzanine boards vs the SRL_{NIEL} is shown. Most mezzanine board components were tested to a dose of 1E13 n/cm². The safety factors which should be applied for NIEL according to ATLAS policy are SF_{SIM}=5 and SF_{LOT}=4. If both safety factors are applied, this gives an equivalent RTC_{NIEL} of 5E11 n/cm² for the mezzanine board electronics. At this level one can see from the plot that about 800 mezzanine boards (out of a total of about 15,000) would receive an NIEL dose above the test level.

In Plot 2, the number of mezzanine boards vs the SRLTID is shown. The mezzanine board components are radiation-tolerant to a level of about 50krad. The safety factors which should be applied for TID according to ATLAS policy are $SF_{SIM}=3.5$, $SF_{LDR}=4$ and $SF_{LOT}=4$. If all safety factors are applied this give an equivalent RTC_{TID} of 700 rads. At this level one can see from the plot that about 1000 mezzanine boards would receive a dose above the test level.

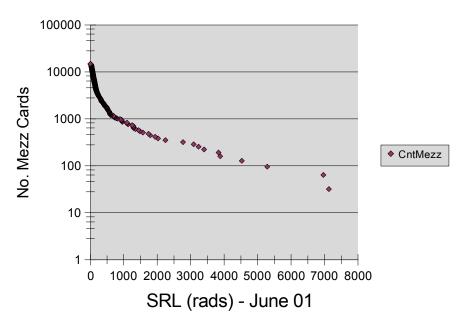
http://atlas.web.cern.ch/Atlas/GROUPS/MUON/layout/MDT-parameter-book.html

² http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm#Radiation%20Constraints

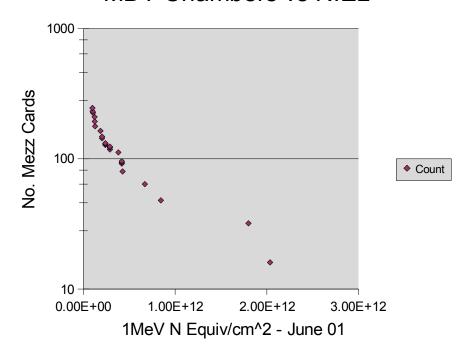
Mezz Boards vs NIEL



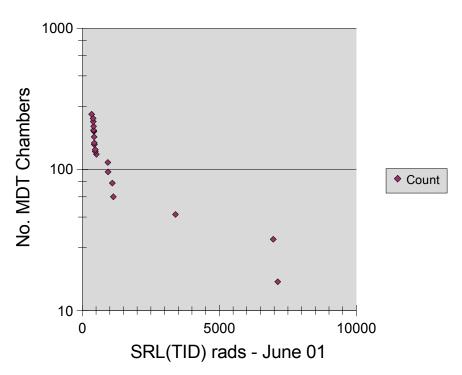
Mezz Cards above TID



MDT Chambers vs NIEL



MDT Chambers vs TID



Action Proposed

It is clear from these results that some action should be taken. The number of affected Mezzanine boards is too high to ignore or to replace. The least costly course of action is to attempt to dispense with some of the safety factors to reduce the number of affected boards to an acceptable level.

For the NIEL case, the only safety factor which is negotiable is SF_{LOT} . If we purchase components from a single lot or small number of lots, and qualify each lot through further NIEL tests, we can eliminate SF_{LOT} . If we consider only SF_{SIM} , the mezzanine boards would tolerate up to $2E12 \text{ n/cm}^2$, which is the maximum SRL_{NIEL} . Thus for NIEL the problem would be solved at the expense of additional testing and procurement overhead.

For the TID case, both SF_{LDT} and SF_{LDR} are in principle negotiable. To eliminate SF_{LDR} for CMOS devices (the limiting device on the mezzanine board is a CMOS voltage regulator) requires annealing for 168 hours at 100° C. This is relatively easy. This increases the maximum SLR_{TID} to 3500 rads. At this level about 200 mezzanine boards would exceed the simulated dose, and only after 5 years of full-luminosity LHC operation. It may be acceptable to plan to replace these boards if necessary.

 SF_{LOT} can be eliminated by the means described above (procurement of homogeneous lots where possible and testing of lots).

In summary, it seems that particular care must be taken to procure COTS components for the mezzanine boards in homogeneous lots and that additional radiation testing must be performed to qualify the lots during production.

MDT Chamber Dose

Plots 3 and 4 show the dose vs number of MDT chambers. This is relevant for the CSM and other per-chamber electronic devices. It should be noted that the level given is at the center of the edge of the chamber with lowest (R, |Z|). This may not be the correct or optimal location for the CSM or other devices.

Appendix- Status of Radiation Testing

The table below lists the current status of radiation qualification tests for all active components on the Mezzanine PCB, as of 5 March 2003.

MDT Component Radiation Test Status (Qualification)

Component	Technology	Test	RTC	Status/Result
MDT-ASD	CMOS	NIEL	1E13 n/cm ²	n/a
		TID	98 krad ³	ok to 300 krad
		SEE	2.5E12 h/cm ^{2 4}	1 SEU/6.4E12 p/cm ² (per device)
AMT TDC	CMOS	NIEL	1E13 n/cm ²	tested
		TID	98 krad	tested
		SEE	2.5E12 h/cm ²	tested
LP3964 V.R.	CMOS	NIEL	4E13 n/cm ²	ok to 1E13 n/cm ²
		TID	392 krad	ok to 60 krad
		SEE	2.5E12 h/cm ²	no SEE to 1.1E13 p/cm ²
TMP36 Temp. Sens.	Bipolar	NIEL	4E13 n/cm ²	not tested
		TID	392 krad	ok to 10 krad
		SEE	2.5E12 h/cm ²	n/a
SN65LVDS179	CMOS ?	NIEL	4E13 n/cm ²	not tested
		TID		ok to 300 krad
		SEE	2.5E12 h/cm ²	0 SEE / 4.6E12 p/cm ² (10 devices)

Simulated Radiation Levels (June 2002) and Safety Factors

Test	SRL	Unit	SF _{SIM}	SF_{LDR}	SF_{LOT}	RTC
TID	7	krad	3.5	4	4	392
NIEL	2.00E+012	N/cm ²	5	4		4.00E+013
SEE	4.00E+011	h/cm ²	5			2.00E+012

 $^{3 \}quad SRL(TID) = 7krad * SF(SIM) * SF(LDR)$

⁴ SRL(SEE) = 5E11 * SF(SIM)