

MDT-ASD Production + QC Plan

DRAFT

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1 Introduction

The ATLAS MDT (Monitored Drift Tube) system consists of about 350,000 pressurized drift tubes of 3 cm diameter, with lengths from 1.5 to 6 m. The MDTs are read out by an octal ASD at one end only. About 45,000 ASD chips are required to instrument the MDT system. With spares we plan to produce and test about 67,000 chips. This document is a draft plan for the production and testing of these devices. We make the following assumptions:

- The current (ASD01A) design is final. We (will) have produced and fully characterized at least 150 prototype devices of this design.
- The production order will be placed through MOSIS, who will handle wafer fabrication, thinning, (optionally) gold backside metallization and packaging.
- All die will be packaged untested (“blind build”). Wafer runs will be screened by MOSIS using their test structures. Preliminary tests based on ~200 chips indicate quite high yield (> 80%), thus the blind-build scenario is more cost effective than wafer level probing.
- Testing, storage and shipment of the packaged devices is the responsibility of the participating institutions.

2 Requirements

2.1 Testing

Each packaged device must be tested to ensure full functionality before installation on a PCB.

2.2 Traceability/Database

The performance of the MDTs depends significantly on characteristics of the MDT-ASD that may vary significantly from channel-to-channel and device-to-device. Currently we anticipate that all “good” MDT-ASD will work satisfactorily in any portion of the detector. However, we plan to serial number each MDT-ASD and record a comprehensive database of measured parameters for possible future use. The database will be accessible via the internet so that the characteristics of any individual channel may be obtained at any time during the commissioning and operation of ATLAS. The database must be backed up at multiple locations for security.

2.3 Maintainability

Because the ATLAS detector is expected to have a greater than 10 year lifetime and because the semiconductor process used for the MDT-ASD is unlikely to be available for more than a couple of years from now, it is necessary to maintain a stock of spare MDT-ASD devices for all anticipated maintenance needs. These devices must be stored under conditions such that they can be used up to 15 years in the future.

3 Parties Involved

Several institutions are participating in the MDT-ASD production effort. The name and role of each is given here. The role of the many other collaborators who have participated in the design of the MDT system and the MDT-ASD is gratefully acknowledged.

3.1 Boston University (BU)

Boston University will issue the purchase order to MOSIS for the MDT-ASD production, and will play a key (but as yet undetermined!) role in the testing. The initial hardware design of the tester was performed partly by B.U. Christoph Posch (christoph.posch@cern.ch) is the technical contact, while Eric Hazen (hazen@bu.edu) is the group leader.

3.2 Harvard University

Harvard University will also play a central role in the MDT-ASD production and testing. Most of the firmware and software for the automatic tester is being developed at Harvard. The final version of the production mezzanine PCB on which the MDT-ASDs will be mounted is designed at Harvard. The group leader is George Brandenburg (Brandenburg@huhepl.harvard.edu). The technical contact is John Oliver (oliver@huhepl.harvard.edu).

3.3 Brandeis University

Brandeis will design and implement the database that will contain the test data. Jim Bensinger (Bensinger@bdhepa.hep.brandeis.edu) is the group leader; Larry Kirsch (Kirsch@bdhepa.hep.brandeis.edu) is the technical contact.

3.4 MOSIS

MOSIS (www.mosis.com) provides IC fabrication and assembly services to government, research and educational customers. They also handle dedicated (production) wafer runs. MOSIS will be the primary vendor for the MDT-ASD procurement.

3.5 CERN

CERN will not play a direct role in this production process, though of course the appropriate ATLAS-sponsored design and production reviews must be completed successfully before production.

4 Production Steps

In this section all steps from design submission to the shipping (or long-term storage) of the MDT-ASDs are described. Details of processing performed by outside vendors is omitted.

4.1 Wafer Production and Packaging

MOSIS will arrange all details of this step. We must provide the following detailed documentation to MOSIS:

- GDS-II file describing our layout. (same as for ASD01A final prototype)
- Bonding diagram:
http://bmc.bu.edu/bmc/asd/asd01a/t0ac_am_pgfp80e_pkg.pdf
- Marking Instructions. Proposed package marking is as follows:

MDT-ASD01A
BMC SEP 02
(Lot number or date code)

A brief summary of the production process follows:

- MOSIS will assemble a reticle site layout from our GDSII file, adding test structures to each site.
- Masks will be manufactured from the MOSIS tape by a subcontractor
- Wafers will be produced from the masks by Agilent
- *Optional:* Wafers will be thinned and backside metallized with gold.
- Wafers will be thinned, diced, packaged and marked by a subcontractor (most likely OSE USA, Inc. of San Jose, CA)
- Packaged parts and excess wafers are shipped to us (Boston University).
- MOSIS retains one wafer from each batch for characterization.

4.2 Receiving

Packaged parts are received at BU/Harvard. A sample of each lot may be opened and tested immediately. Otherwise, the parts will be stored in their moisture-proof bags until testing.

4.3 Serialization

Add devices are serial numbered using a 2-D barcode label before testing. The information on the label is yet to be determined, but at a minimum a unique identifier for the MDT-ASD and a unique serial number.

4.4 Testing

Each device will be tested on a custom-manufactured tester designed by BU and Harvard. The test requires that the operator read the barcode on each device, insert it in a clamshell test socket, and wait for the test to complete (target test time is 10 seconds). The data will automatically be recorded in the test database. Multiple tests of the same device may be performed, and multiple database entries will be made in this case. In order to complete testing of 67,000 devices in a reasonable period, we expect to operate 3 test stations simultaneously. The proposed testing procedure is described in **Appendix A** of this document. The Chip Tester is outlined in **Appendix B**.

4.5 Sorting

Each device will be assigned to a category after testing. A tentative list of categories is:

1. Non-functional
2. Partially functional (at least some channels work)
3. Fully functional, sorted into several “quality grades” according to parametric measurement criteria.

The non-functional devices will be scrapped. The partially functional devices may be useful for bench tests or other non-ATLAS purposes. The fully-functional devices are all possible candidates for use on the detector (even devices outside the parametric cuts could plausibly be needed some years in the future to replace failed devices once the category 4 spares are used).

A significant number of devices will need to be tested to build up a reasonable database before the parametric cuts can be defined for categorization. This may require shipment of initial batches for assembly before the final cuts are defined. It is yet to be determined whether there will be a physical sorting between categories 3 and 4 or just a data sorting.

4.6 Shipment for Board Assembly

The mezzanine boards housing the MDT-ASD chips will be assembled in several batches, possibly at different vendors worldwide. The database will include a record of all shipments of MDT-ASDs, including the quantity, serial numbers, destination, and eventually the serial number of the mezzanine PCB on which the IC was installed.

4.7 Long-Term Storage of Spares

It is planned to produce at least 15% spares (some 6,750 ICs), which must be kept in usable condition until the MDT system is decommissioned, up to 15 years. These will be stored in dry nitrogen in anti-static trays, with sufficient N₂ flow to guarantee that a neutral environment is maintained.

5 Required Resources

Following is a list of the resources required to support the production plan. Note that most of these resources are not be required until completion of the device fabrication,

available well in advance of this date.

Proposed MDT-ASD Production Schedule

7 Summary

A simplified production plan is proposed for the MDT-ASD ICs for ATLAS, based on the observed high process yield and the availability of a fully-automatic, inexpensive chip tester. A single vendor and one shipping step is required. We have the required resources available to complete this plan in the allotted time.

8 Appendix A - Testing

A variety of tests are required to certify each chip as described below, a more detailed description of which is given in the “Chip Tester Users Manual”.

8.1 String test

This is simply the exercising of the 52 bit serial string with test vectors. It is a pass/fail test.

8.2 DC tests

8.2.1 Preamp Inputs

Each channel consists of a pair of pseudo-differential transimpedance amplifiers. The input node of each preamp input sits at approximately 0.8 volts. Both common mode and differential components are measured. Tolerance on the common mode component may be of order ~tens of mv while the differential component is only several mv. The latter is required to avoid building up excessive offsets within the signal chain of each channel.

8.2.2 LVDS outputs

Common mode voltage (~1.2V) and swing (~200mv) must be certified for compatibility with AMT inputs.

8.2.3 Bias generator

Each octal ASD has a bias generator which produces four voltages which are used by all preamps. Current in the bias generator may be altered from its nominal value via external resistor. The bias current is swept over a range of values while the four bias voltages are monitored. The resulting set of curves is fit to a quadratic which yields the values of K_p (transconductance parameter) and V_{th} (threshold voltages) of the nfet and pfets transistors in the bias network. These provide a measurement of typical transistors on the chip and must lie within predefined tolerances.

8.3 Dynamic tests

This is a collection of tests as outlined below, which measure critical performance characteristics of the chip.

8.3.1 Analog pulse shape

While the shaper output pulse is not directly observable, it can be reconstructed by pulsing the chip and time stamping both edges of the discriminated output (TOT mode). Doing this over a range of threshold voltages allows the pulse shape to be reconstructed and the pulse parameters (gain, peaking time) to be extracted.

8.3.2 Discriminator threshold

Similar to Analog pulse shape measurement, a particular discriminator threshold is set and then “found” by varying input pulse height and monitoring the discriminator output. Correct operation of the threshold DAC is verified.

8.3.3 Wilkinson calibration

Wilkinson pulse width is measured as a function of input pulse height, integrator gate width, and rundown current.

8.3.4 Thermal noise rate

The on-chip threshold DAC is varied between normal operating values (negative) through zero and then through positive values while monitoring the discriminator output pulses in TOT mode. Fitting the resulting data to a Gaussian yields an accurate measure of discriminator offsets and thermal noise of the channel. Beyond being a convenient method of measuring offsets, this is a powerful test of correct operation of the entire analog chain. Any significant deviation in preamp operation, shaper gain and/or peaking time, discriminator operation, etc will show up as an abnormal Rate vs Threshold characteristic.

Since rates at high threshold ($> \sim 2\sigma$) are quite low, this test consumes a significant portion (2 – 3 seconds) of the total test time.

9 Appendix B. Chip Tester

The Chip Tester is a small (12cm x 24cm) purpose built unit designed to carry out the testing procedures for the MDT-ASD. The tests described in the preceding appendix result in some 10k bytes of data per chip. The Chip Tester is designed to produce these data with a minimal amount of computer activity, far less than the size of the resulting data block. To satisfy this requirement, the Tester must perform many of the required tests with a high degree of autonomy (firmware).

The Tester has three main sections described below.

9.1 Analog

This contains DACs to supply programmable references for charge injection and bias voltage scans, and ADCs to measure pin voltages.

9.2 Controller

This is an FPGA based controller which receives high level test commands from the computer, interprets them, performs the tests, and returns data to the computer. This allows for very efficient testing of MDT-ASD parameters as the details of the tests reside in controller firmware and not in the PC. For example, threshold voltages are determined by varying input pulse height while monitoring discriminator output. The controller uses a binary search routine and returns the “pulse height at threshold” using a single input command with all intermediate activity resides in controller firmware.

The controller also contains a time-stamp TDC to measure pulse edges (leading and trailing) from the MDT-ASD. The TDC has 2 ns bins and is implemented using the internal DLLs (Delay Locked Loops) of a Xilinx Virtex-II FPGA.

The PC communicates with the tester by means of two fifos called the “Inbox” and “Outbox”. First, the PC dumps the entire list of required commands into the Inbox fifo. This list can be fine tuned by PC resident software. The Controller monitors the Inbox performing one test at a time until empty. The controller returns all test data into the Outbox fifo, encoded with the command ID which produced it. The PC simply monitors the Outbox and reads it until no more data remain.

9.3 Interface.

The PC communicates with the Tester using a standard (National Instruments) PCI digital i/o card with handshaking.

9.4 Throughput

The Device Under Test is inserted into the “clam shell” socket which resides on a daughter card mounted in the tester. The test itself is expected to take less than five seconds or so. The tester GUI will return a result in the form of Functional / Non-Functional along with a “quality grade code” for functional chips. Chips will be sorted and returned to trays accordingly.

Beyond the **5** second test time, we have allocated (conservatively) an additional **15** seconds handling and sorting time as the chip packages have rather fragile leads and operator care must be maintained. The total throughput is thus 3 chips/minute or 180 chips/hr.