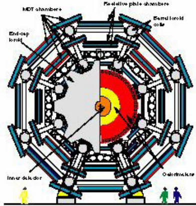

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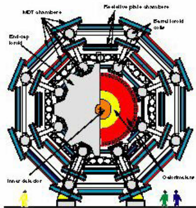
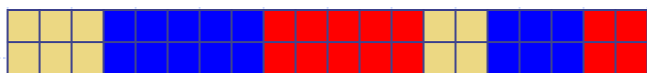
Muon Spectrometer

Quality Assurance, Production Testing, Database

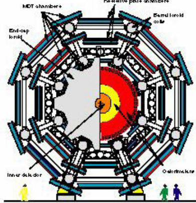
- Chip certification, required tests
- Expected yield
- QA – Test plan
  - ⇒ Production Chip Tester
  - ⇒ Thru-put, manpower
  - ⇒ Data base & tracking through final assembly
- Manpower
  - ⇒ Production management: T. Fries
  - ⇒ Engineering (Including Chip Tester): J.Oliver, E.Hazen, C.Posch, M.Nudell (software)
  - ⇒ Database: L. Kirsch
  - ⇒ Test technicians / students (Harvard, BU)



- Required tests
  - ⇒ Digital functionality : 52 bit serial string register



Shadow register
String register



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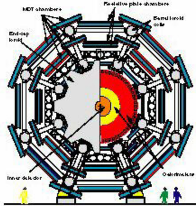
DC tests



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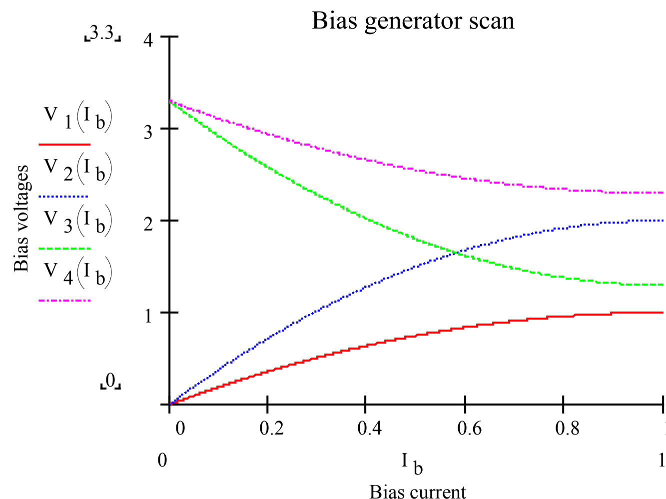
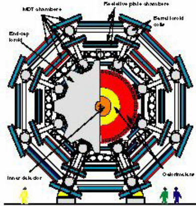
Bias generator sweeps

- Sweep current above and below nominal (0.5 ma) One measurement per chip

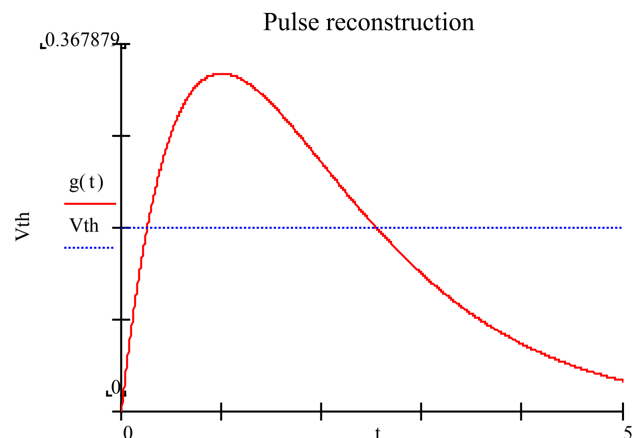


- Quadratic fit gives transistor parameters K_p, V_0 for representative pfet & nfets
- Check "crossover point" for proper bias operation.

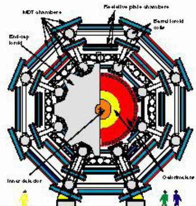


Dynamic Tests

- Pulse testing/cal_inject pulses



- Reconstruct waveform via discriminator V_{th} sweep & timestamping in TOT mode

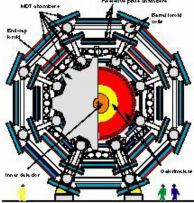


Dynamic Tests (con't)

- Threshold voltage measurement : For fixed threshold, vary input pulse-height to "find" threshold
  ⇒ Determination of disc threshold offsets

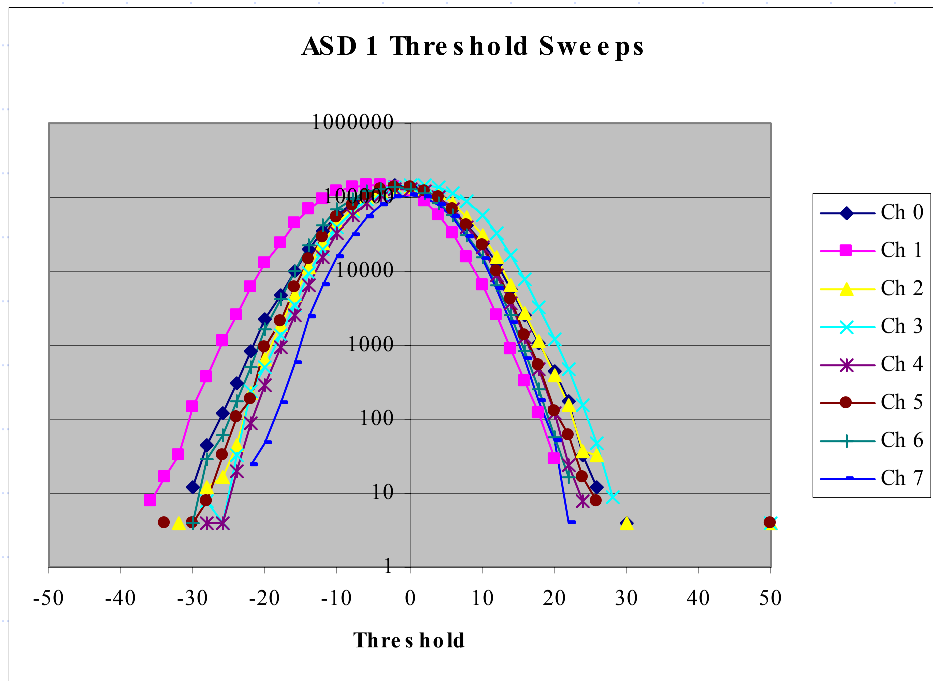
- Deadtime (Wilkinson mode only)

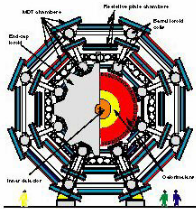
- Wilkinson calibrations
  ⇒ Measure pulse width vs Q_{in}, gate width, & rundown current.



Dynamic Tests (con't)

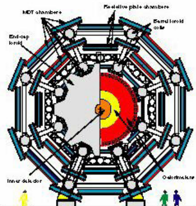
- Thermal noise test – Hit rate vs. V_{th}





- <u>Thermal noise test</u> – Hit rate vs. V_{th}

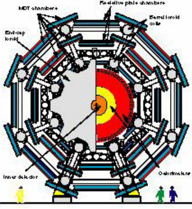
  ⇒ Fit to gaussian
  ⇒ Discriminator offset voltage
  ⇒ V_{rms} noise voltage
  ⇒ Powerful test of entire analog chain
  ⇒ Most analog “faults”…. Preamp gain, shaping time, threshold DAC, discriminator function, ….etc. would yield spurious results.
  ⇒ Can be repeated in-situ on final mezzanine cards.

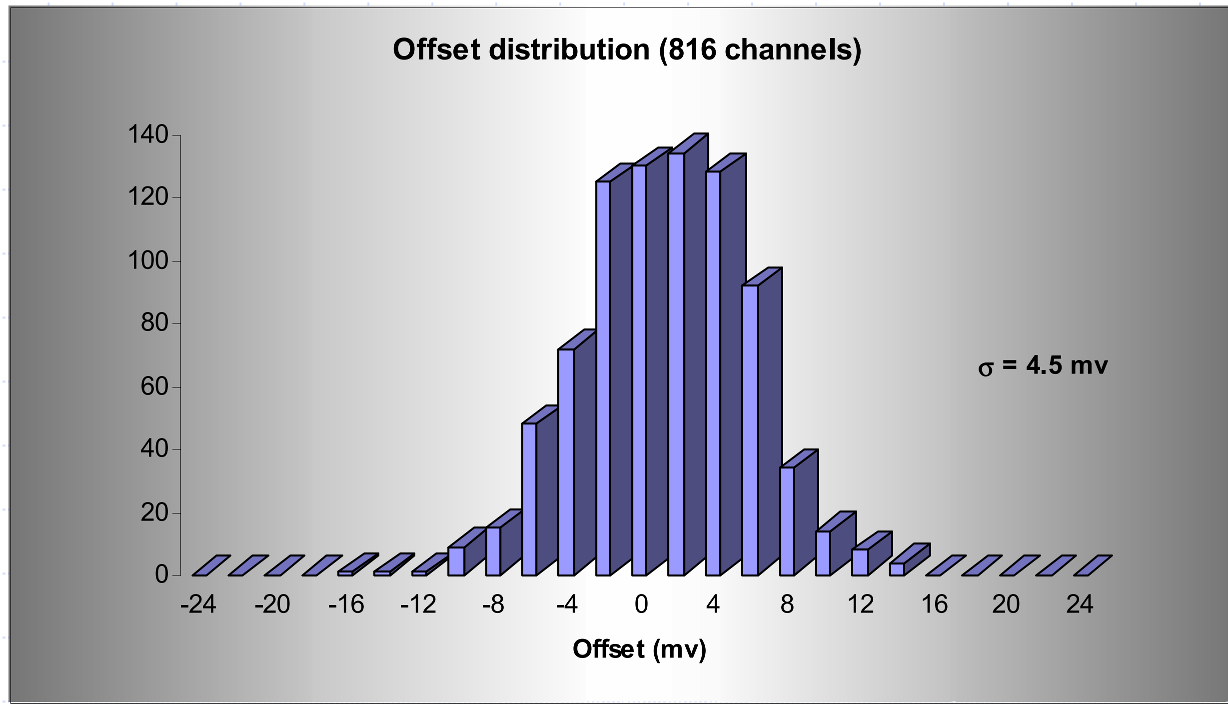


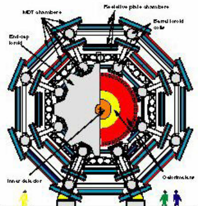
Expected yield

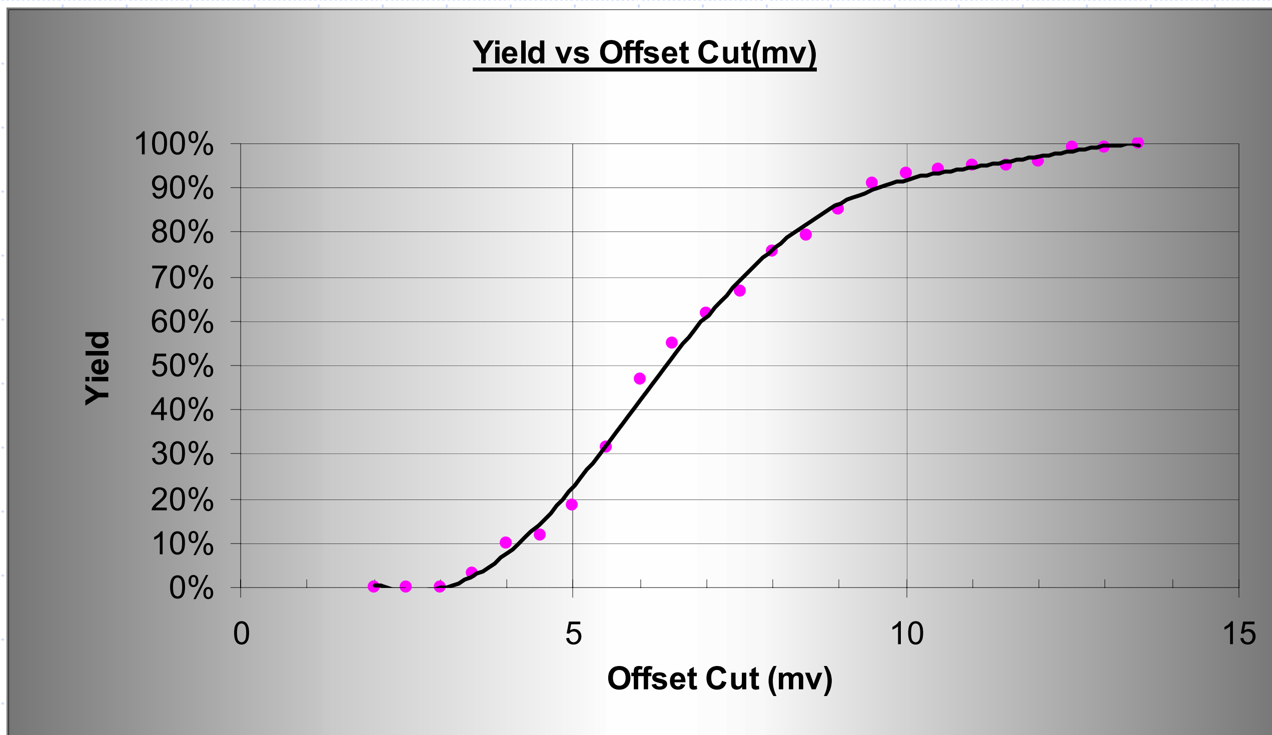
- Based on 200 chips deployed on mezzanine cards
- All chips come from single MOSIS / HP run

  ⇒ 1 single faulty channel observed due to unknown cuase (chip, mezz card, soldering, AMT-2, … ?)
- 100 chips tested in-situ via Noise hit rate test
- Offsets measured on ~ 100 chips (~800 channels)
- Yield estimated via (max-min)/2 offset spread within each chip

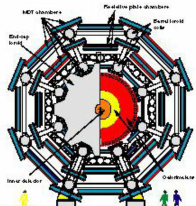



Offset distribution (816 channels)
140
120
100
80
60
40
20
0
-24
-20
-16
-12
-8
-4
0
4
8
12
16
20
24
Offset (mv)
σ = 4.5 mv



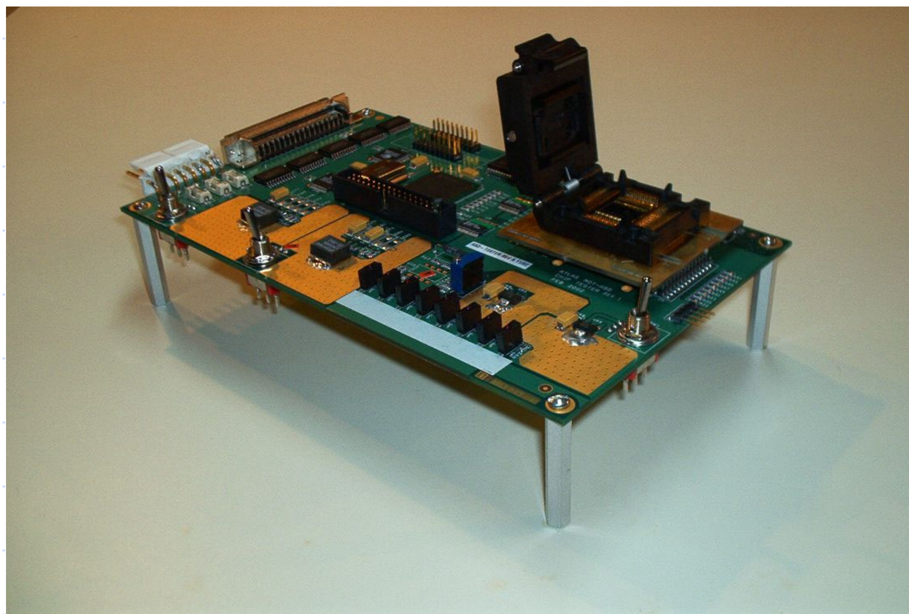


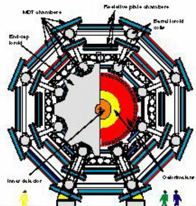
- Likely offset cut ~ 10 mv
  - ⇒ ~ 90% yield
- Remaining chips in ~ 10 mv -15 mv range to be kept as spares
- Production costing based on 80% expected yield



Production Testing

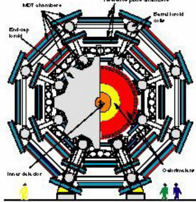
- 67,500 (minimum) chips delivered in vacuum packs
- Opened packages stored in dry nitrogen
- Chips individually numbered & bar coded (2D "Data Matrix")
- Testing done on purpose built MDT – "Chip Tester"





Chip Tester features

- Communicates with PC through 32 bit PCI i/o card
- Low cost device : ~$2k + PC
- Bar code Chip-ID entry
- Performs all string, DC, and Dynamic tests
- Rapid test time 3-5 sec / chip (dominated by thermal noise hit rate test)
- Visual C^{++} GUI
- Database output (Access)



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Chip Tester Architecture

National Instruments PCI Interface Card w/handshake

Inbox Fifo

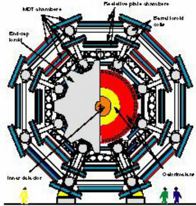
Outbox Fifo

Controller FPGA

DUT

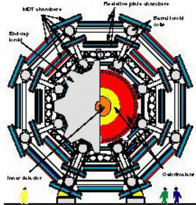
Analog support circuitry

- PC writes high level commands into Inbox fifo
- Retrieves data from Outbox fifo
- Minimal PC i/o traffic : ~ 10k bytes / chip
- Efficient FPGA based algorithms (eg binary searches, etc
- FPGA based (DLL) time-stamp TDC, 2 ns bins (Virtex II)
- Rapid test time (3 –5 sec / chip)



Production Testing

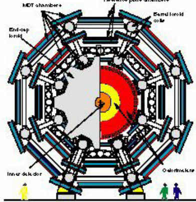
- Plan for ~85k packaged chips (67k + 30% "overage" from MOSIS)
- Multiple Chip Testers (~ 3)
- Assume 5 sec test time + 15 second handling per chip
  - ⇒ 3 chips/min or 180/hr
  - ⇒ 480 hrs total test time
  - ⇒ 12 technician-weeks total (not including "down-time") spread over multiple Chip Testers (Harvard, BU, ?)
- Chips are binned in several "quality rating" trays (according to disc offset and other criteria) returned to dry nitrogen



Database

Larry Kirsch

- Database driven – Microsoft Access
  - No parameters in programs
  - All steps captured automatically in DB
- Server
  - Sharable among multiple stations
  - Accessible remotely
  - Single point of backup



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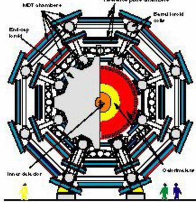

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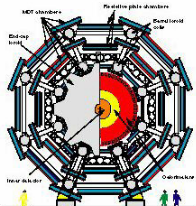
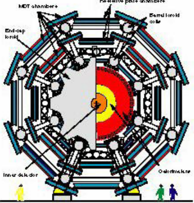
DB Server model

DAQ PC's



Data Base Tables

ASDChanTest	Individual Channel Results
ASDChip	Global Chip Test
RejectCodes	Test Reject Codes
MezzCard	Global Board Tests
FailCodes	Board/Chip Failure codes
QualityParam	Parameters used to assign quality value
RejectParam	Parameters used to Reject chips
RejectParamChanges	History of Reject Parameter changes



Database tables - examples

ASDChip : Table

Field Name	Data Type	Description
IdChip	Text	Bar Code on Chip
Operator	Text	Operator Name
Timestamp	Date/Time	Date/Time of Test
TesterID	Number	Chip Tester ID
String Test	Yes/No	Successful RO of string register (2.0))
Kp	Number	Transconductance Parameter (3.0)
Kn	Number	Transconductance Parameter (3.0)
V0p	Number	Threshold Voltage pfet (3.0)
V0n	Number	Threshold Voltage nfet (3.0)
Ix	Number	Value of Current where V0n=V0p (3.0)
Itotal	Number	Power Supply Current(DC) for whole chip (3.3)
Quality	Number	Quality classification of chip
IdMezzBoard	Text	Bar Code on Mezz Board
RejCode	Number	Reject Code

ASDChanTest : Table

Field Name	Data Type	Description
IdChip	Text	Chip ID
IdChannel	Number	Channel number [0:7]
Vcm_ini	Number	Common mode input voltage (3.1)
DVini	Number	Differential input voltage (3.1)
Vcm_outi_Hi	Number	Common mode output voltage- Hi State (3.2)
DVouti_Hi	Number	Differential mode output voltage- Lo State (3.2)
Vcm_outi_Lo	Number	Common mode output voltage- Lo State (3.2)
DVouti_Lo	Number	Differential mode output voltage- Lo State (3.2)
Voff	Number	Thermal Noise Mean (4.0)
Sig	Number	Thermal Noise Sigma (4.0)
Rate	Number	Thermal noise Rate (4.0)
Vpeak	Number	Analog Monitor Dynamic Threshold (4.1)
Tpeak	Number	Analog Monitor Dynamic Timestamp (4.1)
Vpeak_ext	Number	Dynamic Threshold via external calibration injection capacitors (4.2)
Tpeak_ext	Number	Dynamic Timestamp via external calibration injection capacitors (4.2)
Voff_calc	Number	Threshold Offset Voltage. Should equal Thermal noise value (4.3)
A_Disc1	Number	Disc1 Hysteresis Linear fit A*X+B (4.4)
B_Disc1	Number	(4.4)