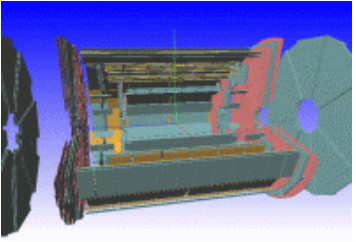
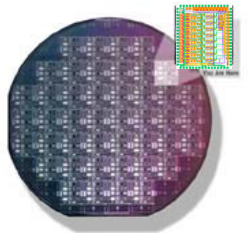
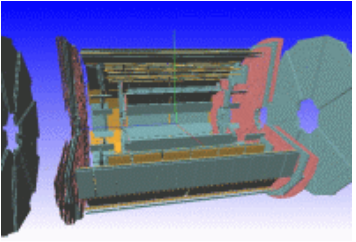




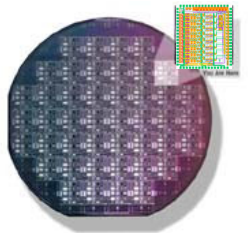
ATLAS MDT-ASD

Integrated Circuit Production And Testing Plan

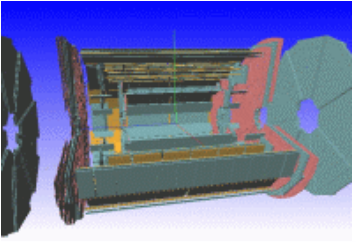
E. Hazen – Boston University



Chip Production Plan
Overview

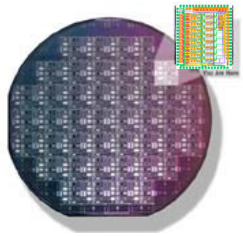


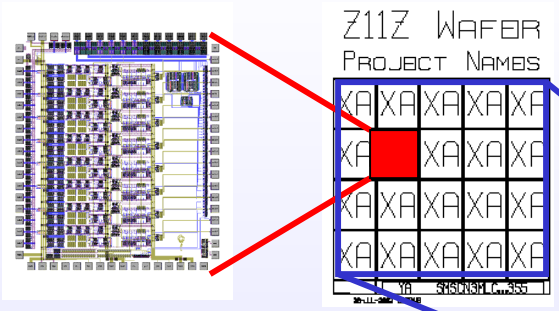
- Packaged devices purchased through MOSIS
- No wafer/die level testing
- Packaged devices tested by us on custom-made automatic tester
- Database of key parameters kept; devices serialized
- Generous (15%) spares allotment kept in storage indefinitely (dry N_2) for repair/replacement

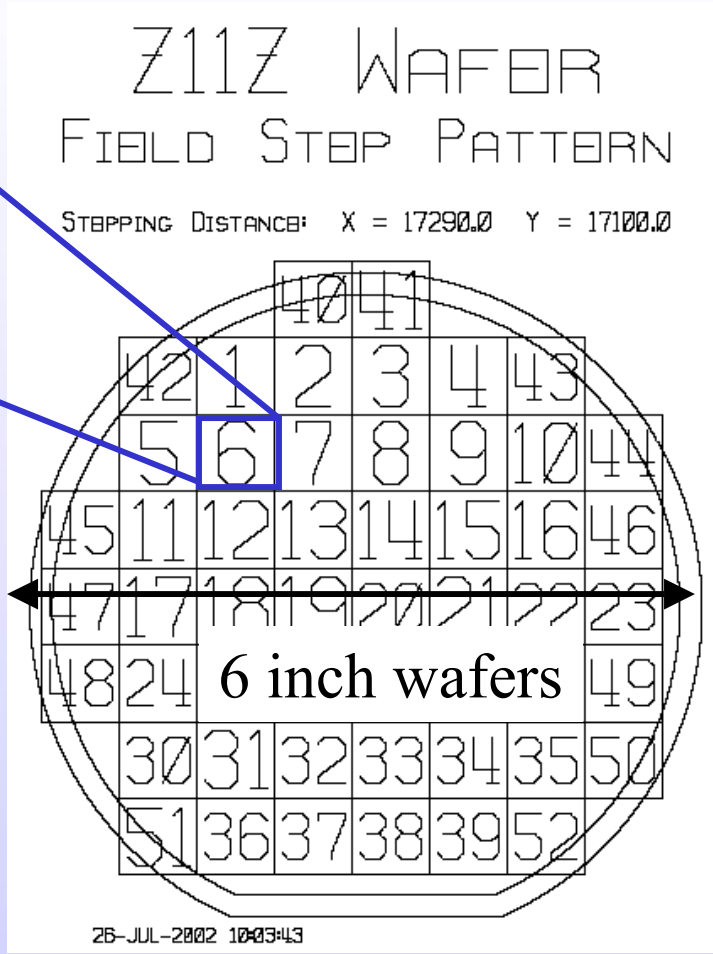


Chip Production Plan

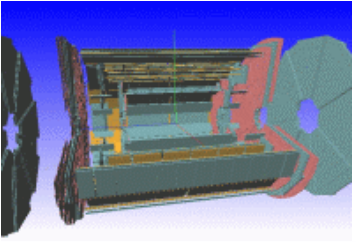
Wafer Layout



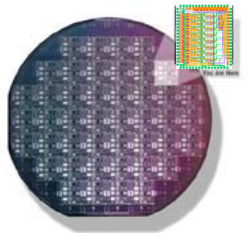




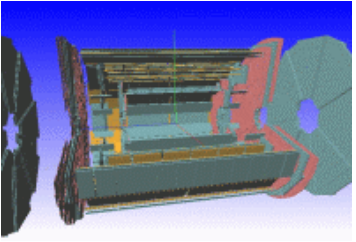
- Agilent AMOS14TB process (0.5 µm)
- Die size 3.2 x 3.9 mm
- 5 x 4 die per field
- 45 fields / 900 die per wafer



Chip Production Plan
Wafer/Chip Yield

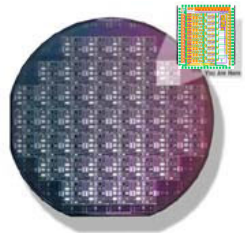


- Wafer Yield
  - 25 wafers started per lot
  - 15 good wafers *guaranteed* per lot
  - MOSIS expects to ship 20 wafers
    - Our estimates based on 15 wafers are likely quite conservative
- Die yield
  - 90% based on test of 100+ devices
  - Others' experience with this process is similar
    - We use 80% yield to be conservative

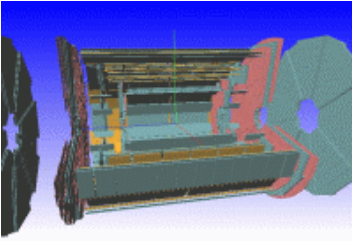


Chip Production Plan

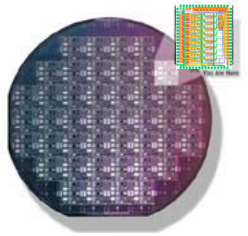
Estimate of Quantity Required



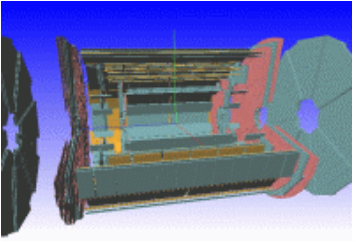
Installed ASDs	45000	15000	Mezz PCBs
Spares (on PCBs)	3%	450	spare PCBs
Spares (not mounted)	15%	6953	spare ICs
Assumed IC Yield	80%		
Total ICs required	**66629**		
ICs per lot (15 wafers)	13500		
ICs delivered (minimum)	**67500**	**5**	**Lots required**
Ics delivered (likely)	90000		



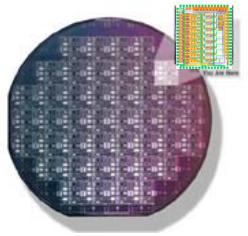
Chip Production Plan
Fabrication Steps



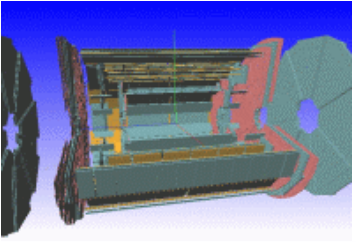
- GDS File sent to MOSIS
  (identical to final prototype file)
- MOSIS arranges production:
  - Layout of reticle site with 20 identical chips
  - Manufacturing of mask set
  - Wafer fabrication at Agilent
  - Wafer qualification using test structures
  - Shipping of finished wafers to packaging vendor
- Delivery of packaged ICs to us



Chip Production Plan
Post-Production Processing

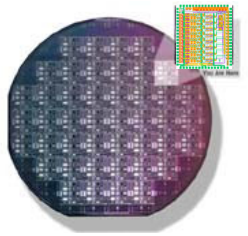


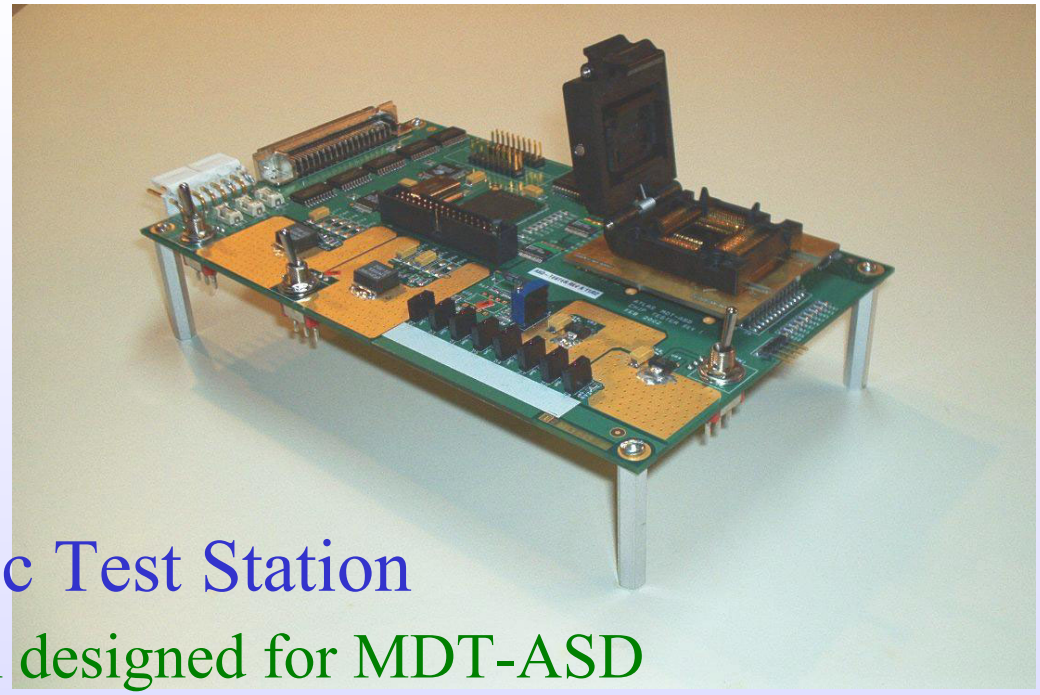
- Receive parts in sealed bags / trays
- Unpack and serialize (barcode labels)
- Test in automatic tester
  - Assume throughput of 3 chips/minute (3-5 sec test)
    - Total test time about 10 man-weeks
  - Record all parameters in database
  - Categorize:
    - Not Functional, Partially Functional
    - Fully Functional; several “Quality Grades”
- Store in dry nitrogen before assembly
- Seal in moisture-proof bags for shipment to assembly house



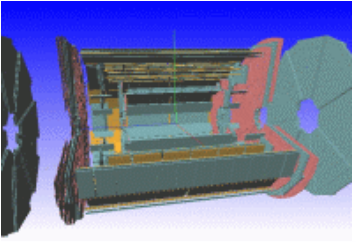
Chip Production Plan

Automatic Tester



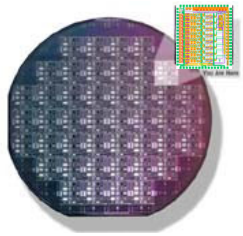


- Automatic Test Station
  - Custom designed for MDT-ASD
  - Full AC/DC Test in 3-5 sec
  - All parameters recorded directly in database
    - More details to follow!

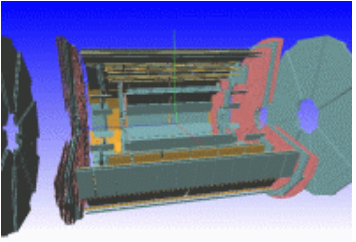


Chip Production Plan

Schedule

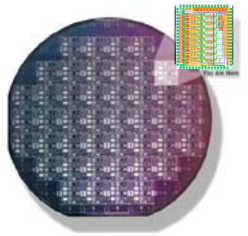


		2002				2003			
		Sept	**Oct**	**Nov**	**Dec**	**Jan**	**Feb**	**Mar**	**Apr**
Order Placed	1-Oct-02								
Fabrication	12-14 Weeks								
Testing	6-8 Weeks								
MDT Schedule									



Chip Production Plan

Preliminary Quotation



Qty	Item	Unit	Total
1	Mask Charge	$55,000	$55,000
5	Lot of 15 (min) wafers	$42,000	$210,000
1	Packaging	$60,000	$60,000
	Total for 67,500 parts		**$325,000**

Cost per (untested) IC	$4.81
Cost per good IC	$6.02
Cost/IC initially installed	$7.22

(Previous estimate was $335,000 total)