ASD-lite review @ BNL
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This document briefly describes ASD-lite, a simplified 4 channel Preamp/Shaper/Discriminator for use in testing of prototype MDT chambers. The chip is to be produced in quantity up to 10k channels. The purpose of the review is to solicit technical input on all aspects of the design; muon chamber signal processing, technical aspects of CMOS implementation, and details of circuit design and layout.

1 General

1.1 Overall description

1.1.1 MDT chambers

Length :	up to 6 meters
Dia :	30 mm
Wire dia:	50 u
Wire resistance	44 ohms / meter
Impedance (Z_0)	370 ohms
Termination	370 ohms in series with 470 pf
AC coupling cap	470 pf

1.1.2 Drift gas

The original baseline drift gas was $Ar/N/CH_4$ which is a well behaved linear drift gas. When using this gas we expect "classic" tail behavior with inverse time relation. Unfortunately, this gas has aging properties insufficient for use in ATLAS and was replaced by the non-linear Ar/C02. *ASD-lite has been optimized for the now-abandoned linear drift gas.*

1.1.3 On-chamber pc boards

The ASD chips are mounted on a "mezzanine" card which is in turn connected to a chamber mounted "hedgehog" card. Each mezzanine card will contain six ASD-lites for a total of 24 channels per mezzanine / hedgehog combination. The hedgehog contains no active circuitry except for input protection diodes.

1.1.4 ASDs

The ASD topology follows the U. Penn pseudo-differential input scheme and is shown in upper level schematic on pages 4 & 5 of schematic/layout appendix. Each MDT connects to a "signal" preamp with an associated "dummy" preamp. The dummy preamp input connects to the mezzanine card but goes no further. Following the pseudo-differential pair of preamps is a diff-amp which produces a fully differential signal and provides some gain.

Following this are two stages of diff-amps which comprise a shaper implementing a "classic" positive ion tail cancellation. The shaper output is ac coupled to a final gain stage and then to a discriminator and LVDS output cell.

1.1.5 Changes from previous design submissions

Previous design submissions had utilized the pseudo-differential input structure with single ended internal stages. This resulted in a topology which allowed particularly fast peaking time of final shaped pulse of ~ 8ns. Experimentally, however, this class of devices proved unstable when mounted on chamber. Oscillations in the range 100 – 200 MHz were observed and no viable means was found for making operation of these devices unconditionally stable.

A second major problem was on-chip crosstalk which existed at the level of several percent. Several components of crosstalk were observed: analog (linear) and digital. The digital component was attributed to substrate coupled noise.

To address these issues, the ASD98b submission incorporated several key changes.

- Preamp / bias circuit redesign for greater PSRR. This suppresses possible instability due to feedback through the power supply lines
- Separation of on-chip *ground* and *substrate* connections. This reduces or eliminates possibility that digital ground bounce will couple to the substrate and then to analog sections
- Separation of preamp power/gnd connections from those of subsequent stages (crosstalk reduction)
- Design was made *fully differential* end to end (crosstalk reduction and stability)

On chamber tests of ASD98b were highly successful from the point of view of crosstalk and stability. Input protection, however, was found to be insufficient. ASD98b chips would not survive chamber sparks or "screwdriver test" in which hv coupling cap is discharged intentionally. *The ASD99a submission, received in late March 99, has substantially increased input protection, but is otherwise identical to the ASD98b.*

1.2 CMOS process

1.2.1 General

Process is HP 0.5 micron nwell triple-metal CMOS available through MOSIS. There is a linear capacitor option consisting of polysilicon over an active ndiffusion in an nwell. The process is silicided yielding very low polysilicon and diffusion resistivities. There is a "silicide" block layer available which allows exclusion of silicide over polysilicon but not over diffusion. This is used primarily for well behaved polysilicon resistors. Operating voltage is 3.3 volts.

1.2.2 Process specs

	n-channel	p-channel	either
Minimum gate length			0.5u
Threshold voltage (typ)	0.76	0.88	
Kprime (ua/V^2)	92	26	
N+ diff sheet res	2.2	2.2	
Poly sheet res (silicided)			2.0 ohm/sq
Poly sheet res (silicide blocked)			90 ohms/sq
Gate oxide thickness			~100A
Gate capacitance			~ 3.5 (ff/u^2)
Linear capacitor			~ 2.3 (ff/u^2)
Vbkd	11.3V	-9.6V	

2 Circuit details

2.1 Preamp

2.1.1 Specifications

- Power dissipation ~ 3.3mw per preamp (~ 1 ma @ 3.3V)
- Zin ~ 120 ohms (dc & ac/dynamic)
- Input noise density ~ $1.3nV / \sqrt{Hz}$

2.1.2 Description

The preamp is an unfolded cascode shown on page 6. Its input transistors M1 (a & b) operate at a nominal 1 ma standing current total. Transistor M2 constitutes the cascode and current is supplied to the "high impedance" node via a cascode current source (M4 & M3). There is a 10k load resistor (R2) on the high impedance node which, along with R1 and R3, sets the low frequency part of the input impedance. The feedback resistor is divided into two parts, R1 and R3, and is effectively their parallel combination. The reason for this is dc considerations. Operating at 3.3 volts requires upper and lower transistors in this configuration to operate near the rails. Output voltage, taken from high-Z node, should be ideally near Vdd/2 or 1.6 volts. The parallel connection of R1 & R3 achieves this operating point.

2.2 Differential amplifiers

Each of the differential amplifies Da1 through Da4 is of the same basic design shown on page 8. The basic amplifier is a differential pair of transistors, M3 & M4, with gain set by load resistor shown externally (see page 4) and source impedance (R1 plus transistor source impedances) . The common mode output operating point is established by common mode feedback. The output nodes, OUTB (OUTA) are connected to the gates of M7(8) and M9(10) respectively. These transistors, M[7:10] are operating in their linear region as resistors with, typically, 50 – 100 mv across them. Common mode gain is achieved by modulating these fet resistances via common mode output voltage. The gain of this loop is of order 10 or so. The circuit works by driving the common mode output voltage close to the voltage Vref (Vdd/2).

Bandwidth of each of the diff-amp stages is limited by load resistance and the total capacitance of the output node consisting of the parallel capacitance of output transistor drains, traces, and gate input of subsequent stage. Typically, each stage incurs a pole at a time constant of about 4 ns with an 11 Kohm load (~ 40 MHz 3db bandwidth per stage)

Since gain of each diff-amp is largely determined by the ratio of load to source resistance (silicide blocked poly) , the gain is desensitized to process variation.

2.3 Shaper

The shaper is composed of two stages of pole/zero embedded in the diff-amps Da[2:3]. Shaping is standard $1/(t+t_0)$ with $t_0 = 10ns$. Peaking time at the shaper output is 12 – 15 ns.

The shaper output is ac coupled to one additional diffamp referred to as pre-discriminator gain stage. This stage has smaller load resistance and no source resistance, hence, higher gain and bandwidth at the expense of higher process variation of gain. Since the threshold is applied at its input however, the gain sensitivity to process variation is irrelevant.

2.4 Discriminator

The discriminator, shown on page 17, is a high-gain differential amplifier, with symmetrical, current-mirror loads. The main diff pair (M1, M2) is biased at 400uA. Two current-mirror "loops" provide a differential output at VOUT, VOUTN. The voltage gain is about 500 with no hysteresis.

Hysteresis is provided by (M1A, M2A) which unbalance the static current through the main diff pair by a variable external current, shifting the effective discriminator threshold by up to 100mV. Positive feedback from two inverters drives (M1A, M2A)

The main bias current is provided by R1 (poly). The expected operating regime is at a threshold of about 20 primary electrons, which corresponds to a differential signal of about 300mV at the disc input.

2.5 LVDS output cell

This cell, shown on page19, provides an "LVDS-like" low-level logic output, with a nominal swing of 200mV differential into 100Ω centered at 1.2V. This corresponds to the "reduced range link" described in IEEE 1596.3.

Differential drive is provided directly from the discriminator outputs to two moderately-sized inverters. These inverters drive the output stage, which is essentially a pair of inverters (M10/13 and M16/18), with their output current limited by transistor pairs operating in their resistive region (M9/15 and M17/20). Common-mode feedback from the outputs to the current-limiting FETS sets the common-mode output voltage.

The DC characteristics are set entirely by transistor sizes and are thus subject to process variations. Observations on a small number of fabricated devices largely agrees with Monte Carlo simulations and is compatible with the intended TDC.

2.6 Analog output

Analog output is provided for channel 0 only. The pad driver cell is shown on page 21 and is simply a set of cascaded source followers reminiscent of the old

"Damn Fast" parts from National Semi. The gain of this cell is only about 0.5 when driving Hi-Z. It is capable of driving a terminated twisted pair but at lower gain. Still, it is useful as an observation of MDT signal shape and also for noise measurements.

2.7 Input protection

As mentioned earlier, the ASD98b had extremely minimal input protection and would not survive chamber sparks without substantial off-chip protection in the form of multistage resistor/diode networks. The ASD99a was submitted with substantially larger esd protection diodes.

The ASD-lite preamp design is such that the input pad is connected to gate polysilicon and to the preamp's feedback components. It is anticipated that the primary damage mechanism in this case, is gate oxide breakdown of the input fets. Gate oxide breakdown for this process could be expected to be of order +/- 8 volts or so. Thus, the job of the input protection scheme is to maintain the input transistor gate to within this limit. To do this efficiently in a standard bulk CMOS process, we need input protection diodes with large periphery and minimal area resulting in small series resistance.

Primary input protection is provided by a pair of large n+ diodes, labeled nd400, and a series 3Ω input resistor. The resistor is a silicide blocked polysilicon resistor attached directly to the input pad. Each nd400 diode consists of eight fingers of n+ diffusion, 50 microns each, surrounded by p+ diffusion for a total finger length of 400 microns. The whole structure is surrounded by an additional n+ diffusion which acts as the collector of an npn structure. The collector scoops up current discharged into the substrate more effectively than the p+ cathode strips alone. Each nd400 has a total capacitance, area plus fringe, of about 0.8 pf.

There is also a smaller pair of p+ diodes connected to the positive supply rail. In principle, a human body model type discharge into these diodes would dump current into the positive supply rail which, therefore, requires a clamp for bare chip handling. This clamp is based on the UMC "Corner" design found on the MOSIS web site, but is a bit simpler. It is by no means, guaranteed to withstand a full HBM discharge while the device is unconnected.