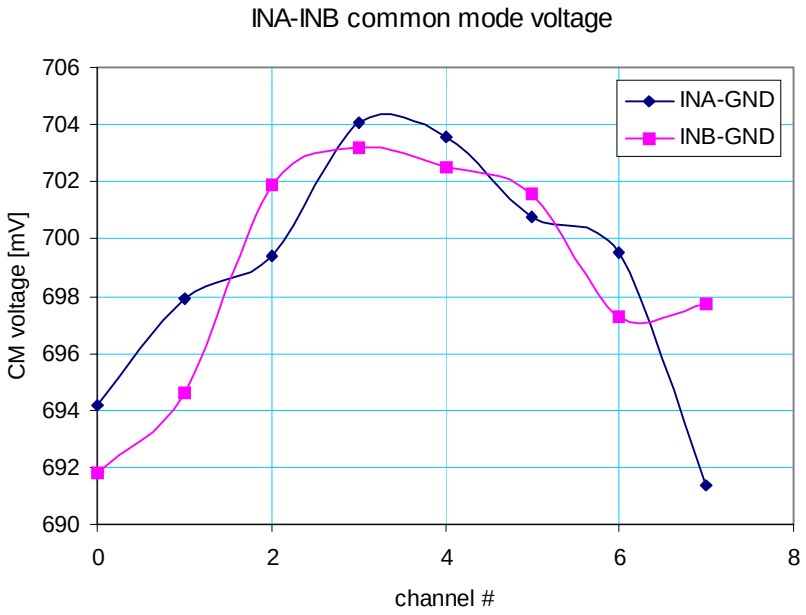
ASD01A lab test report

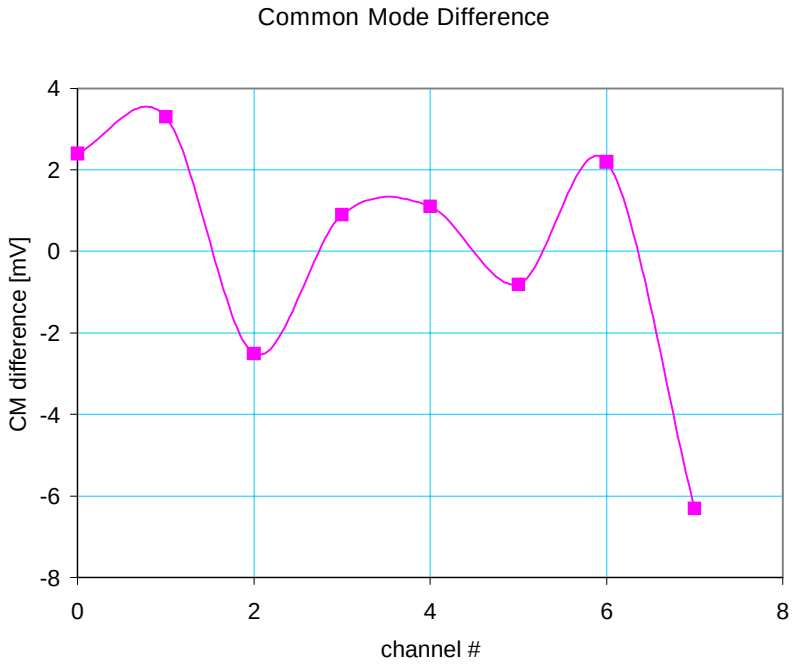
C. Posch, CERN, 13 Aug. 2001

1. DC Tests

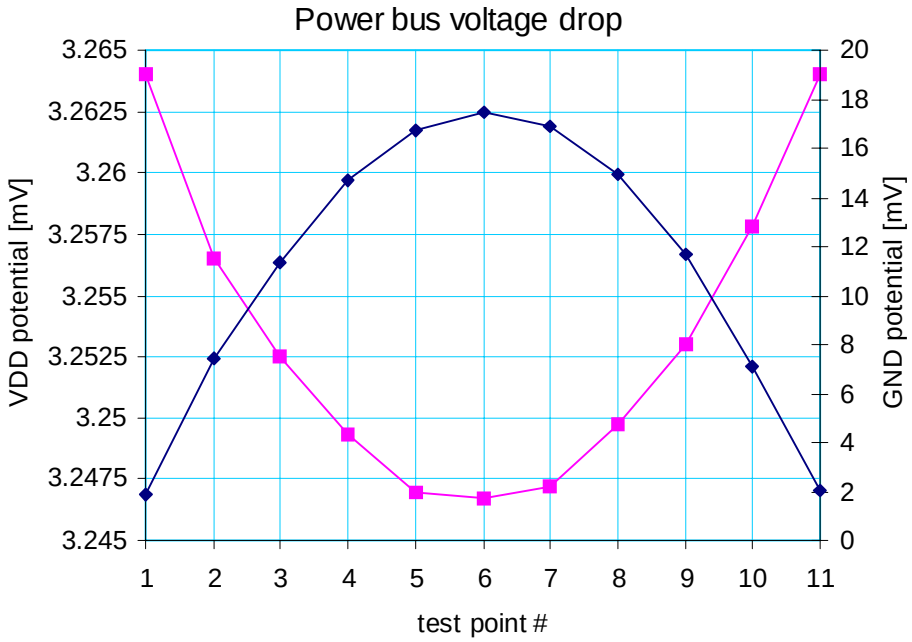
1.1 Pre-amp input common mode

Pre-amp input node (INA, INB) voltages referred to ground measured for all channels at nominal supply.





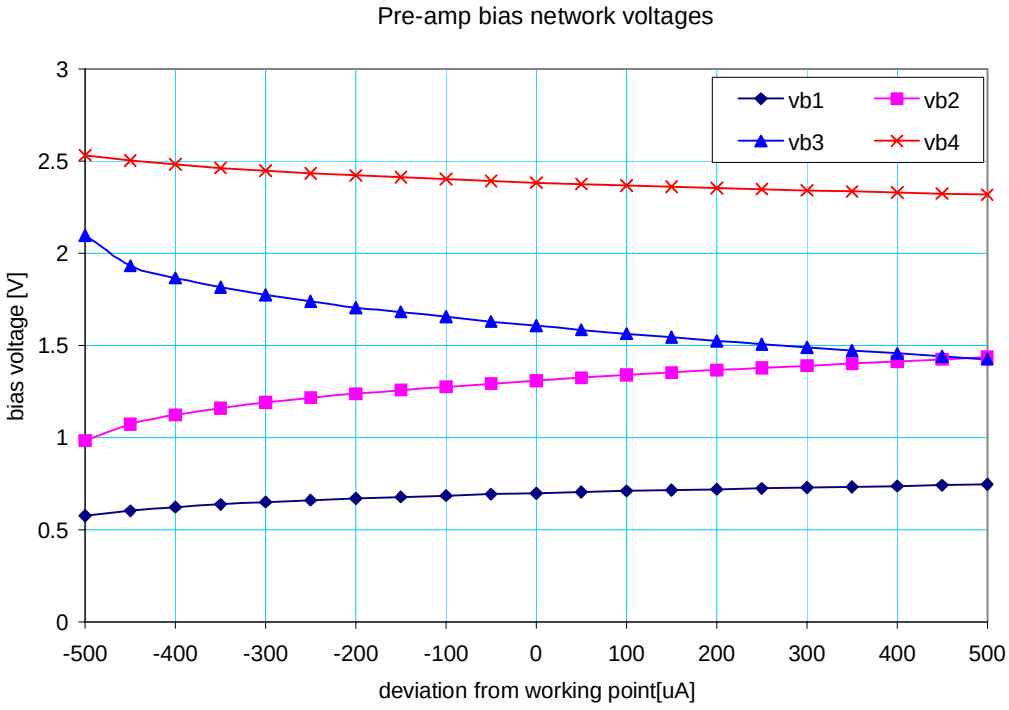
1.2 Power bus voltage drops



VDD and Ground levels, measured at designated probe points along power bus VDD-1, GND-1 which supply the pre-amplifiers. The maxima of the voltage drops are below 20 mV.

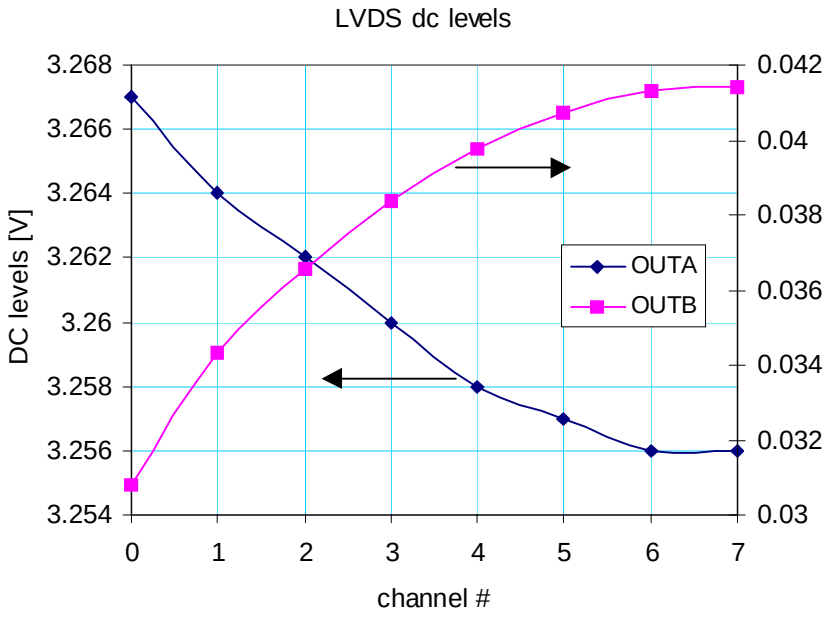
Similar measurements with comparable results exist for the other power buses. (Also compare to 1.1 and 1.4)

1.3 Pre-amp bias network



VB1 - VB4 measured referred with respect to GND. Current (x-axis) swept into VB2 node.

1.4 LVDS output DC levels

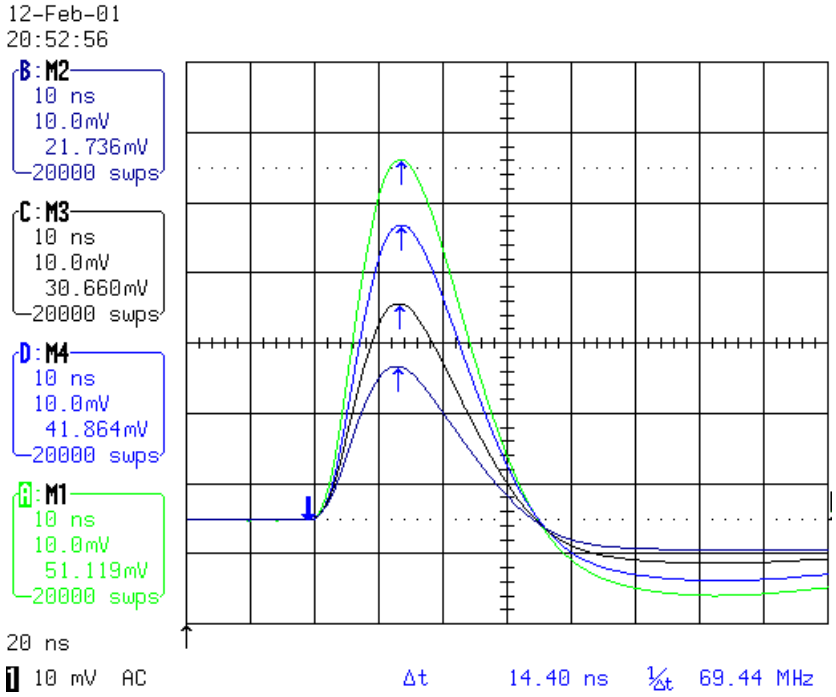


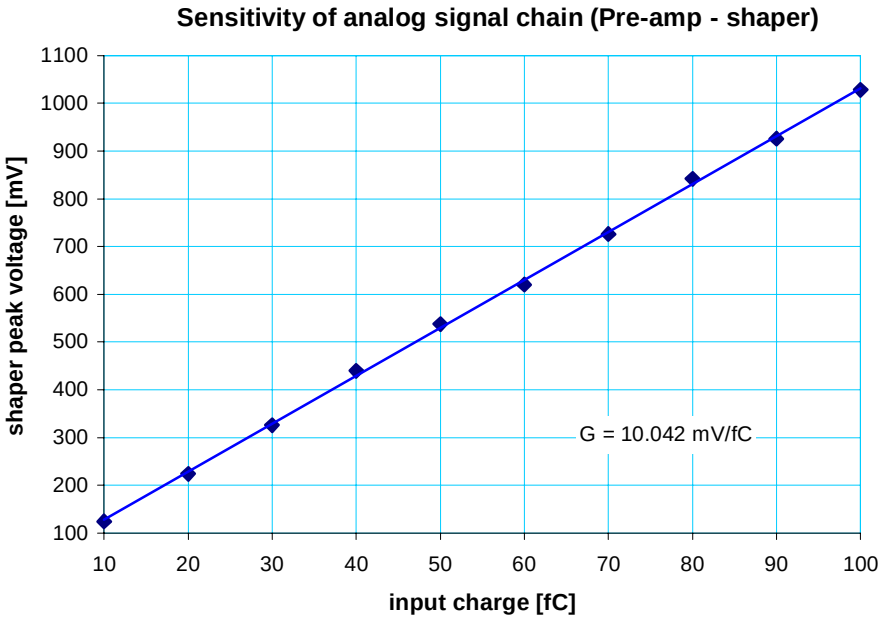
Note that during this measurement, the second pair of power pads at opposite side of die (bottom, at CH7) were not bonded!! The maximum drops with the pads connected are expected to be smaller by a factor 4.

2. Pre-amp - Shaper

2.1 Gain and sensitivity

Oscilloscope traces of the shaper output at the threshold coupling point. The measurements were taken with a calibrated probe using well defined input charges. The peaking time (time between the arrows) is 14.4 ns. There is a probe attenuation of 10:1 which is not accounted for in the peak voltage values in the left hand column. Due to the differential architecture, the voltages have to be multiplied by a factor 2 to obtain the total gain.

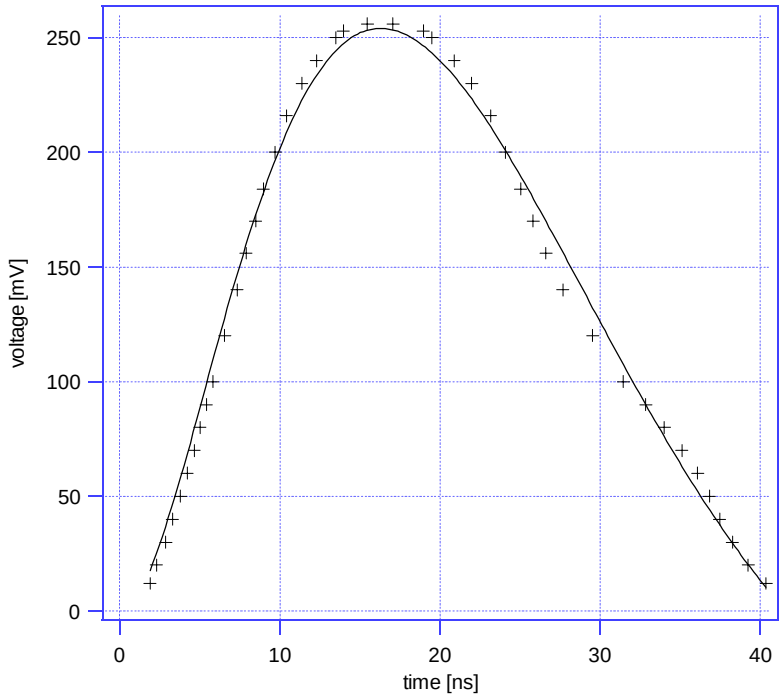




Calibrated shaper output peak voltage vs. pre-amp input charge curve of the pre-amp - shaper combination. The sensitivity is slightly above 10 mV/fC and shows excellent linearity.

2.2 Pulse shape

From the outside (without using a probe station) the pulse shape at the discriminator input can be reconstructed by combining the data from measurements of types 3.3B) and 3.4 at zero discriminato hysteresis (compare also 3.5)



The continuous line in the plot is a bipolar fit to the measurement points. The bipolar function in its general form can be expressed as

$$g(s)=\frac{n!s\tau}{(1+s\tau)^{n+2}} \quad \leftrightarrow \quad f(t)=\left(1-\frac{t/\tau}{n+1}(t/\tau)^n e^{-t/\tau}\right)$$

with the peaking time

$$t_p=\tau\cdot\left(n+1-\sqrt{n+1}\right)$$

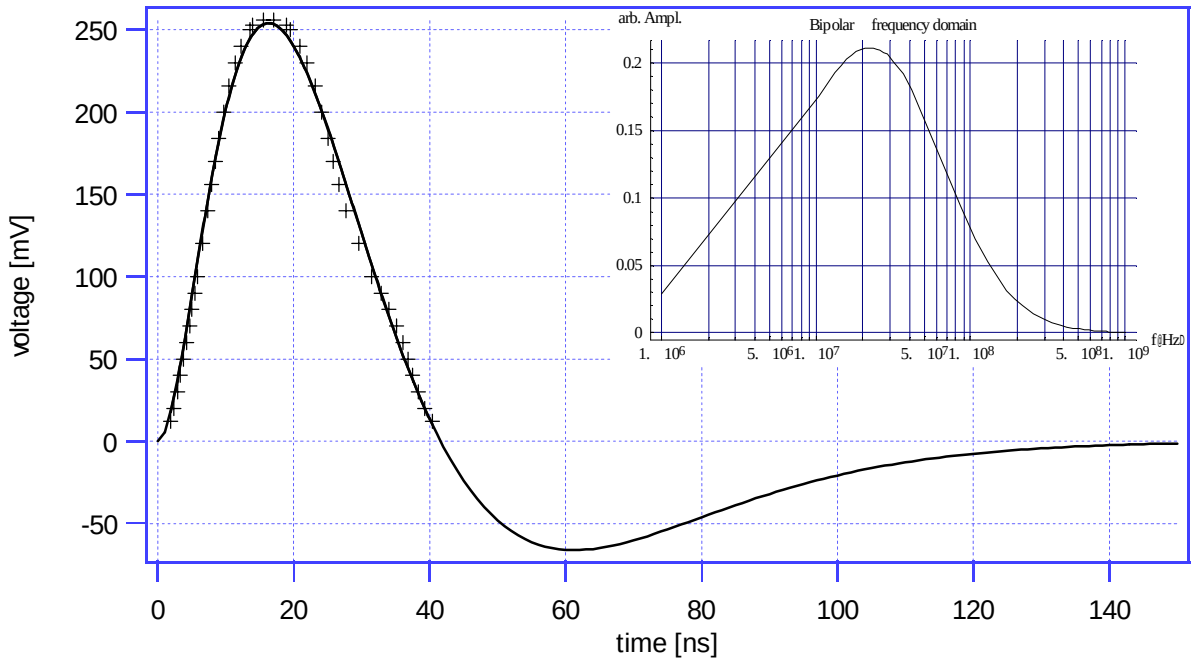
Setting n = 2 gives the used fit function in the time domain:

$$K0\cdot t^2(1-K2\cdot t)\cdot e^{-K1\cdot t}$$

The fit to the measurement points yields the coefficients: K0 = 6.11038, K1 = 0.0832564, K2 = 0.0240536

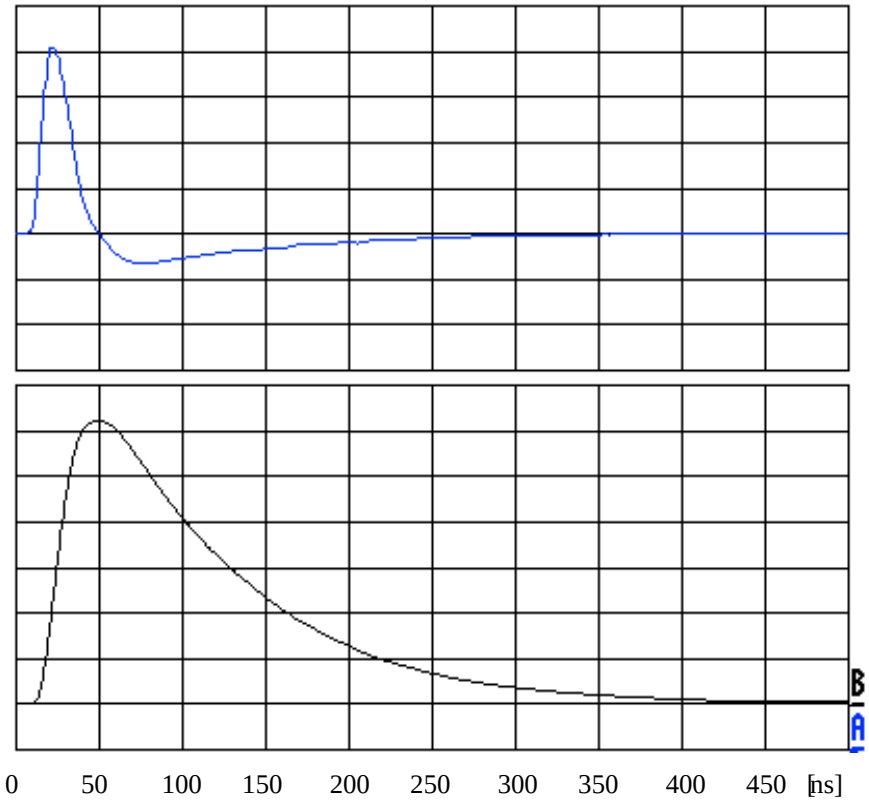
and K1 yields the peaking time $t_p=\frac{1}{0.0832564}\cdot\left(3-\sqrt{3}\right)=15.229\ ns$

The function plotted over a wider time range shows the complete pulse shape (including the measurement points):



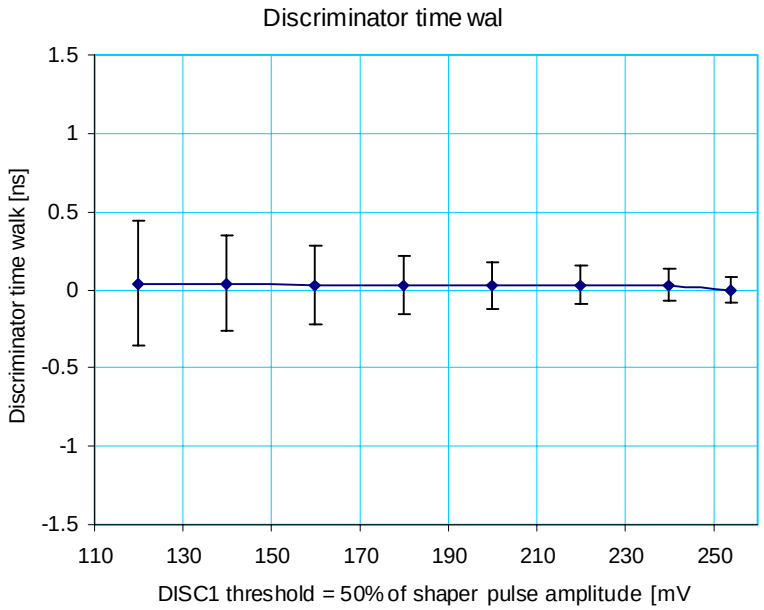
2.3 Baseline return

Oscilloscope traces of the shaper delta impulse response (top) and its integral (bottom). The bipolar shaped pulse achieves area balance after ~ 400 ns.



3. Discriminator

3.1 Threshold DAC linearity and range

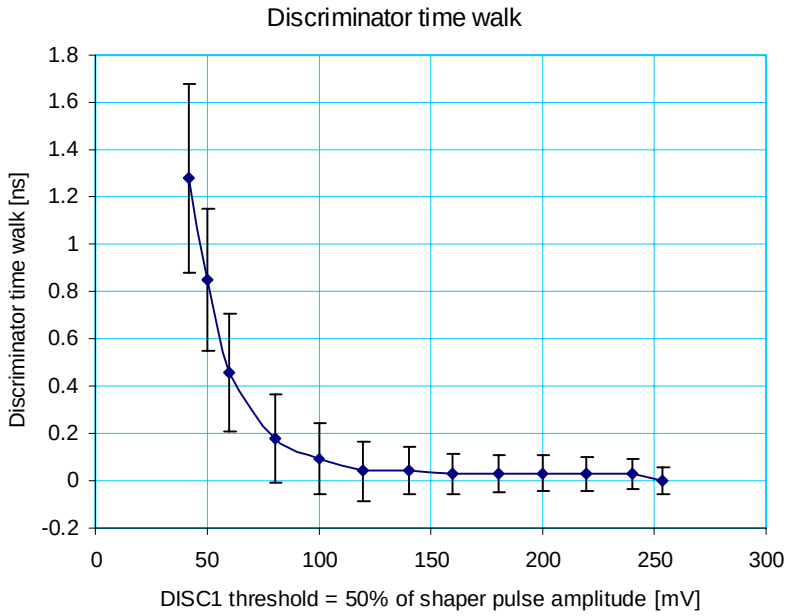


Threshold and input pulse amplitude are swept simultaneously. Pulse amplitude set to 2 times threshold (threshold at 50% point of pulse edge). For sufficiently large signals where discriminator time walk is negligible, Threshold DAC linearity and range appear perfect.

For discriminator time walk (= expanded range plot see following section 3.2).

3.2 Discriminator time walk

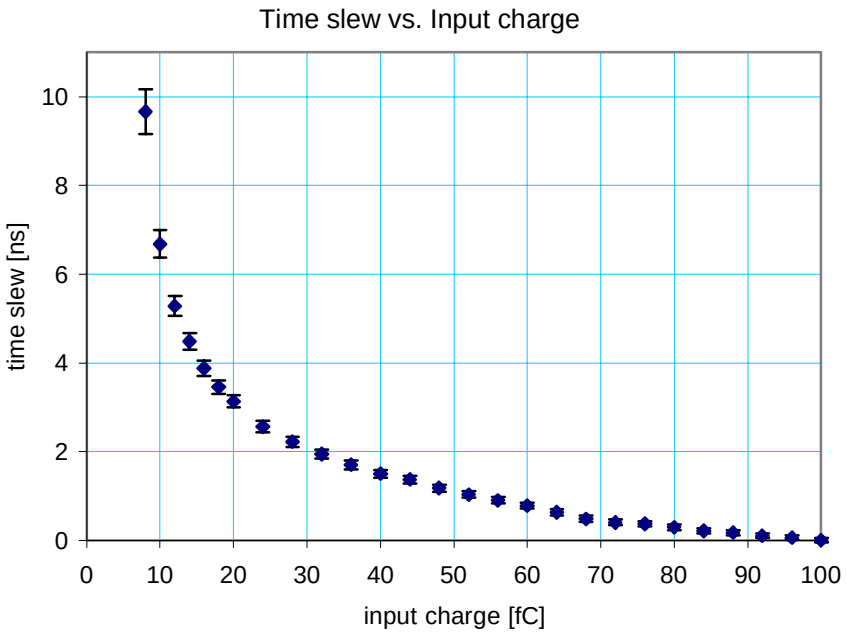
This time slew is generated in the discriminator itself - small signals do not drive the discriminator to change state as fast as large signals do - and must not be confused with "time slew" which results from the moving trigger point caused by the varying slew rate due to different signal strength (see section 3.3).



Threshold and input pulse like in 3.1. Discriminator time walk as a function of signal strength/threshold (constant ratio). The error bars give the sigma of the discriminator fire time distribution (800 - 60 ps).

3.3 Time slew

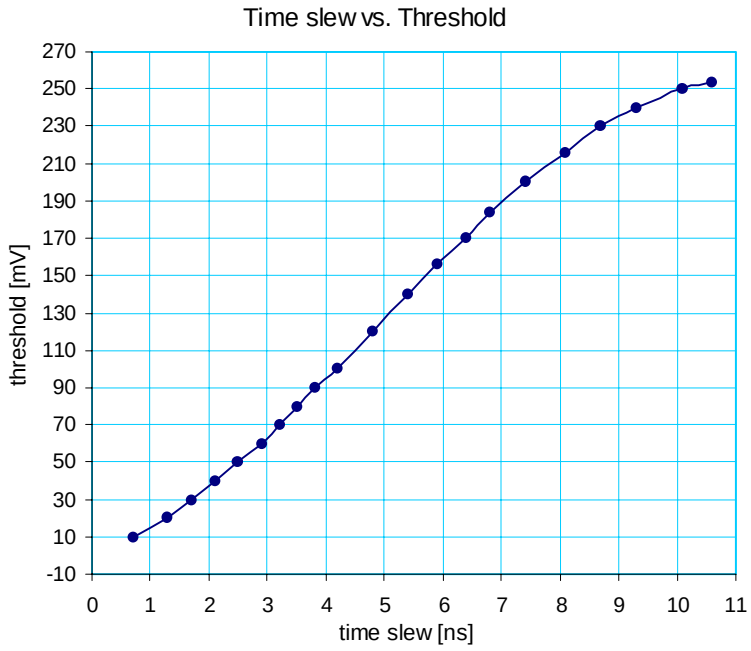
A) Time slew vs. input charge



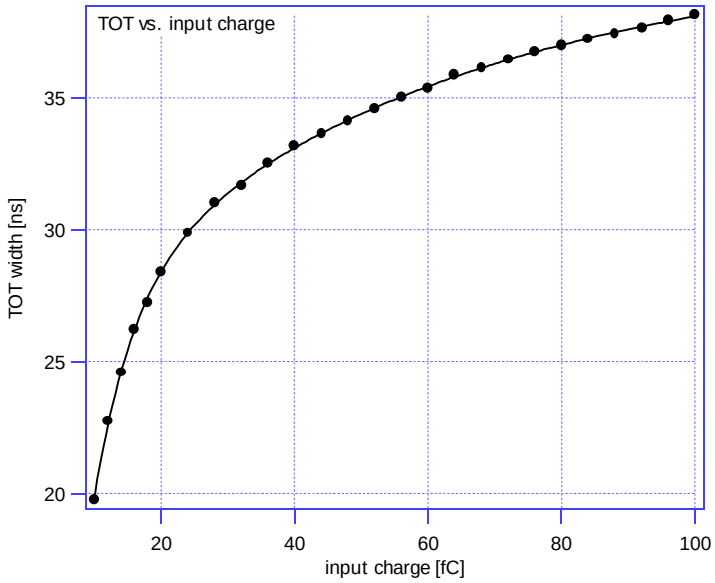
Time slew is measured for nominal threshold (60 mV), sweeping the signal charge from just above threshold to ~ 10 times threshold. This is the real time slew and is a combination of discriminator time walk (section 3.2) and shift in firing time due to varying signal amplitude and slew rate. The error bars are again a measure of the sigma of the discriminator timing and range from 1 to 0.1 ns.

B) Time slew vs. threshold

The time slew is measured for a fixed signal, sweeping the threshold from noise level to above the pulse peak. In other words, the rising edge of the pulse at the shaper output / discriminator is scanned. Pulse shape and peaking time can be extracted from the data (compare 2.2 and 3.5).



3.4 ToT versus threshold overdrive



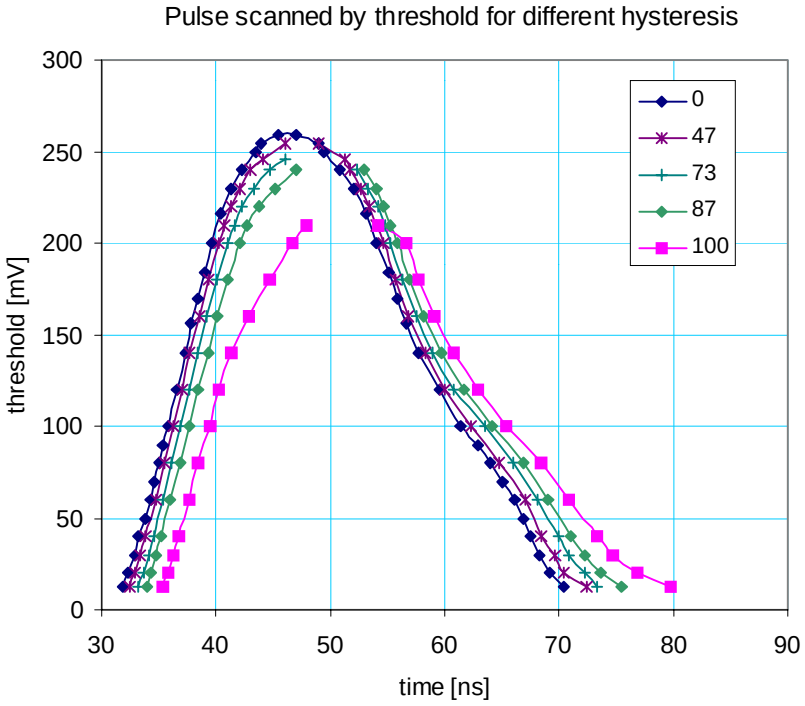
Width of ToT pulse as a function of signal charge for nominal threshold (60 mV); no discriminator hysteresis. The continuous line is a double exponential fit to the measurement points using the fit function:

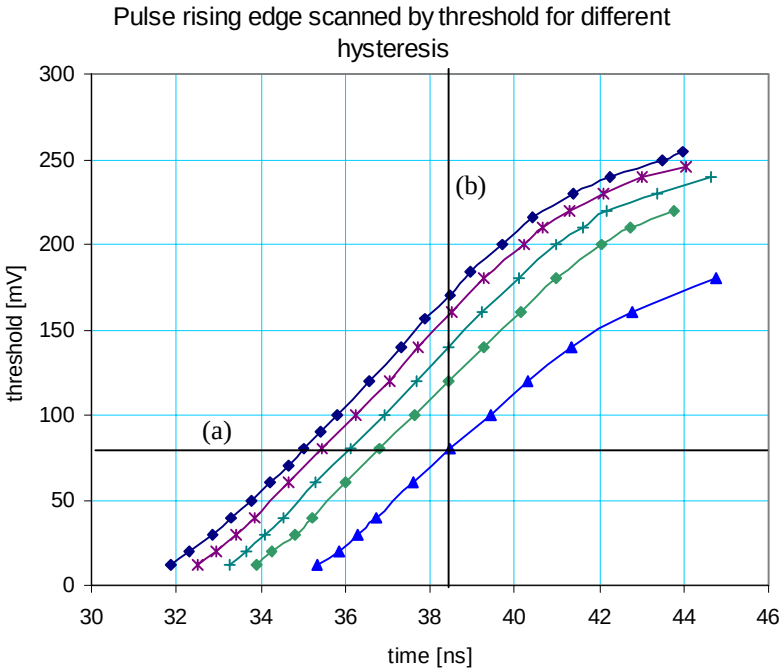
$$f(x) = K0 + K1 \cdot e^{-K2 \cdot x} + K3 \cdot e^{-K4 \cdot x}$$

with coefficients K0 = 40.458, K1 = -15.479, K2 = 0.018759, K3 = -42.761, K4 = 0.17035

3.5 Hysteresis

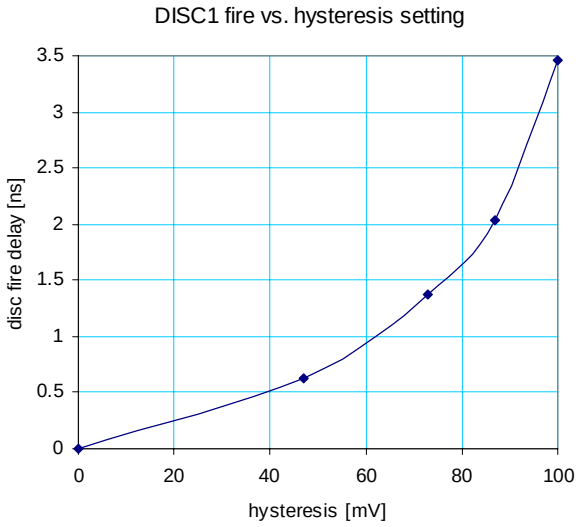
Combining 3.3B) and 3.4 allows for looking at the complete pulse shape. Scanning identical shaper pulses with different settings of hysteresis shows the influence of the hysteresis on the discriminator action. The plot shows curves for 0, 47, 73, 87 and 100 mV of hysteresis.



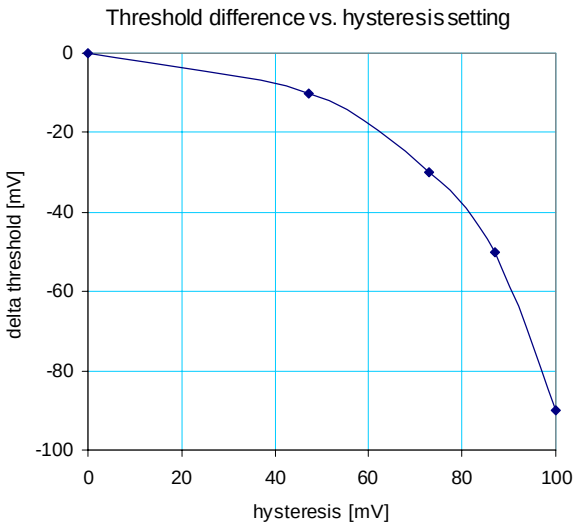


Looking at the rising edge only one can determine (a) the shift in discriminator firing point as a function of the hysteresis setting and (b) the change in threshold voltage necessary to achieve the same firing point fo varying hysteresis settings (true threshold) referred to the threshold at zero hysteresis.

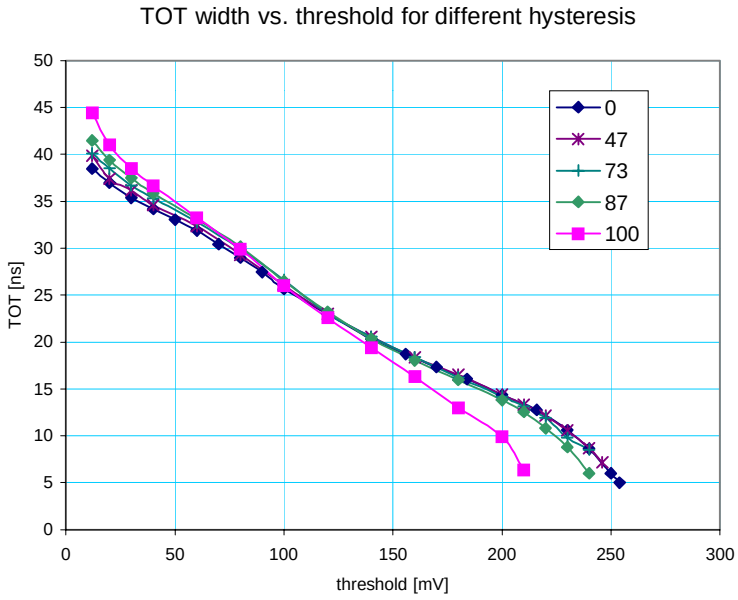
All measurements in this section where done with one relatively small input signal of ± 240 mV (STR-STRB) into 50 fF injection capacitor (corresponding to 24 fC) which results also in a ~ 240 mV or a bit bigger signal at the shaper output (threshold coupling point); Pre-amp-shaper gain: ~ 10+ mV/fC. Therefore this signal covers approximately the nominal range of the threshold DAC (0 - 255 mV).



(a)



(b)

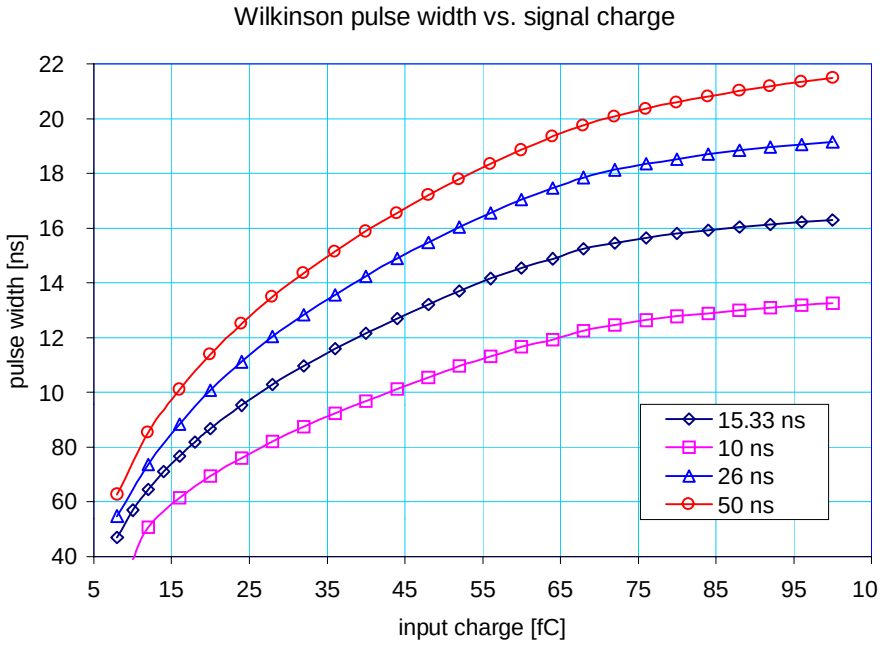


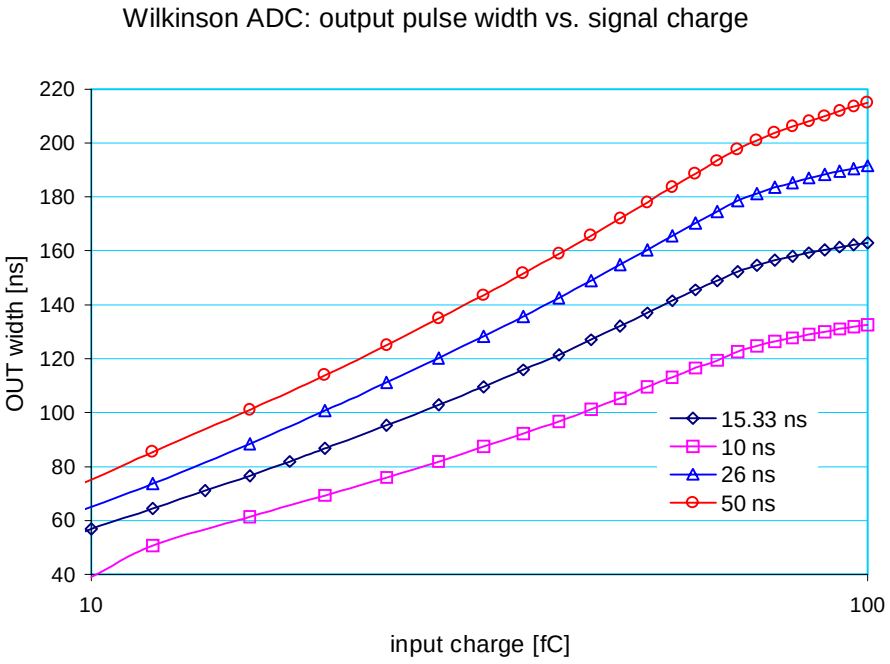
The influence of the hysteresis on the discriminator action can also be illustrated by plotting the ToT width for different hysteresis settings as a function of the threshold for a constant input signal.

4. Wilkinson charge ADC

4.1 Transfer characteristic

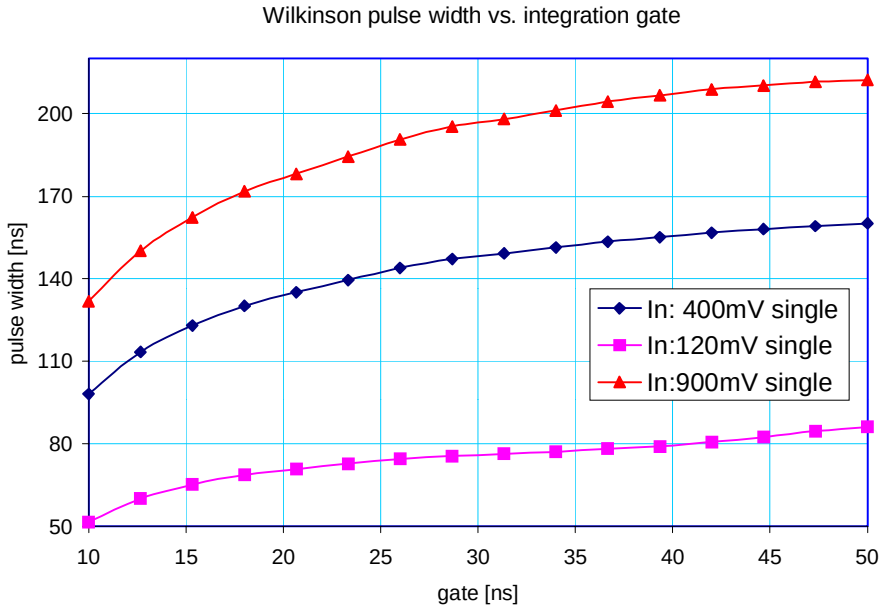
The transfer characteristic of the Wilkinson charge-to-time converter (output width vs. input charge) fo different integration gates.



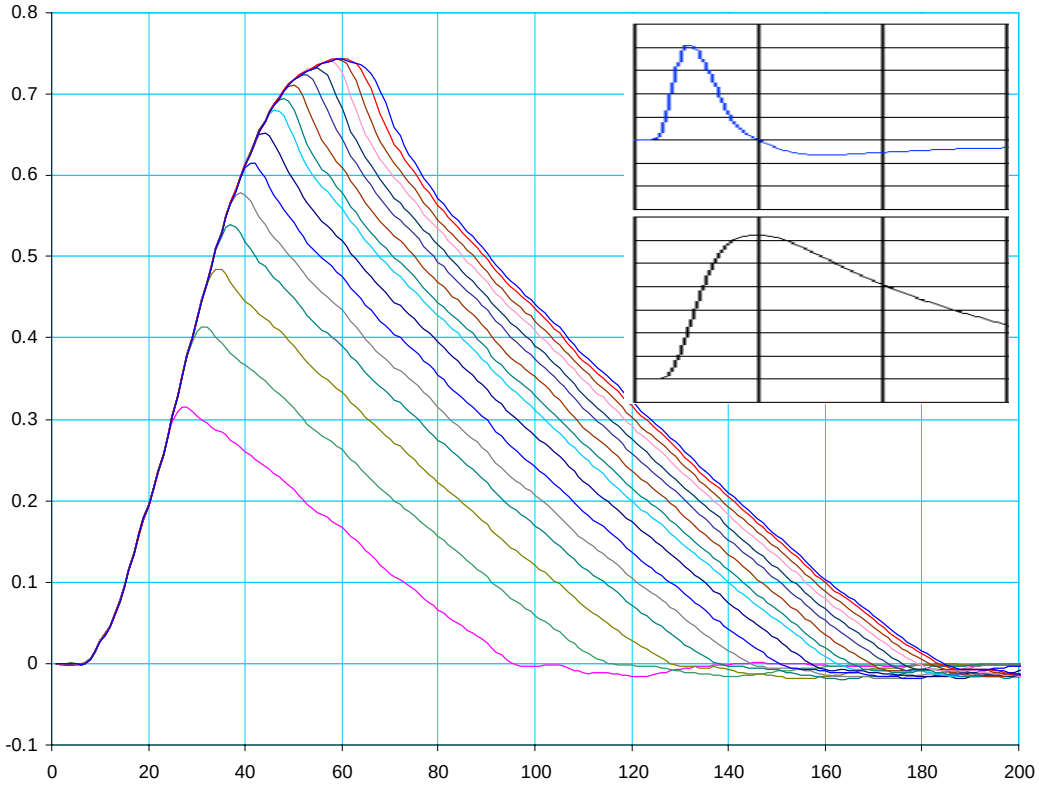


Same data plotted on a log scale.

4.2 Integration gat

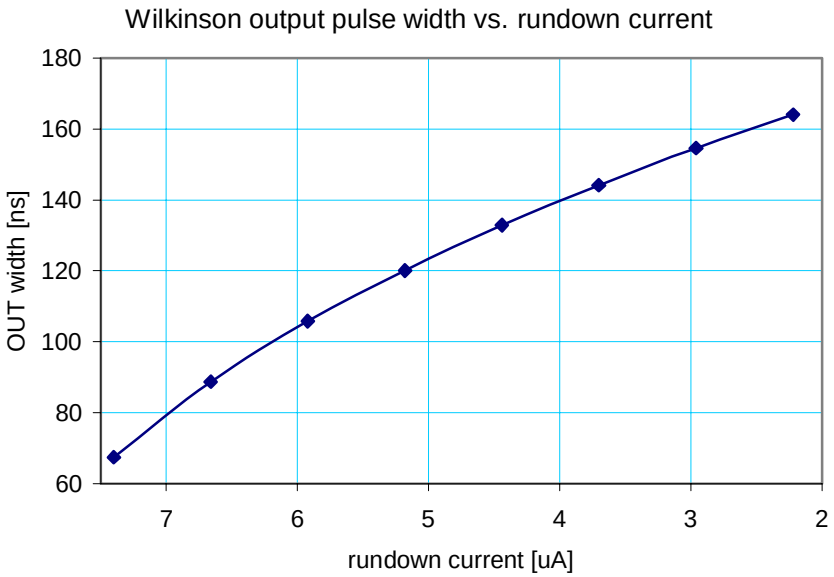


3 signals (120, 400, 900 mV single, steps into 50fF), Wilkinson pulse width vs. integration gate. The gate is swept over its full range from 10 - 50 ns.

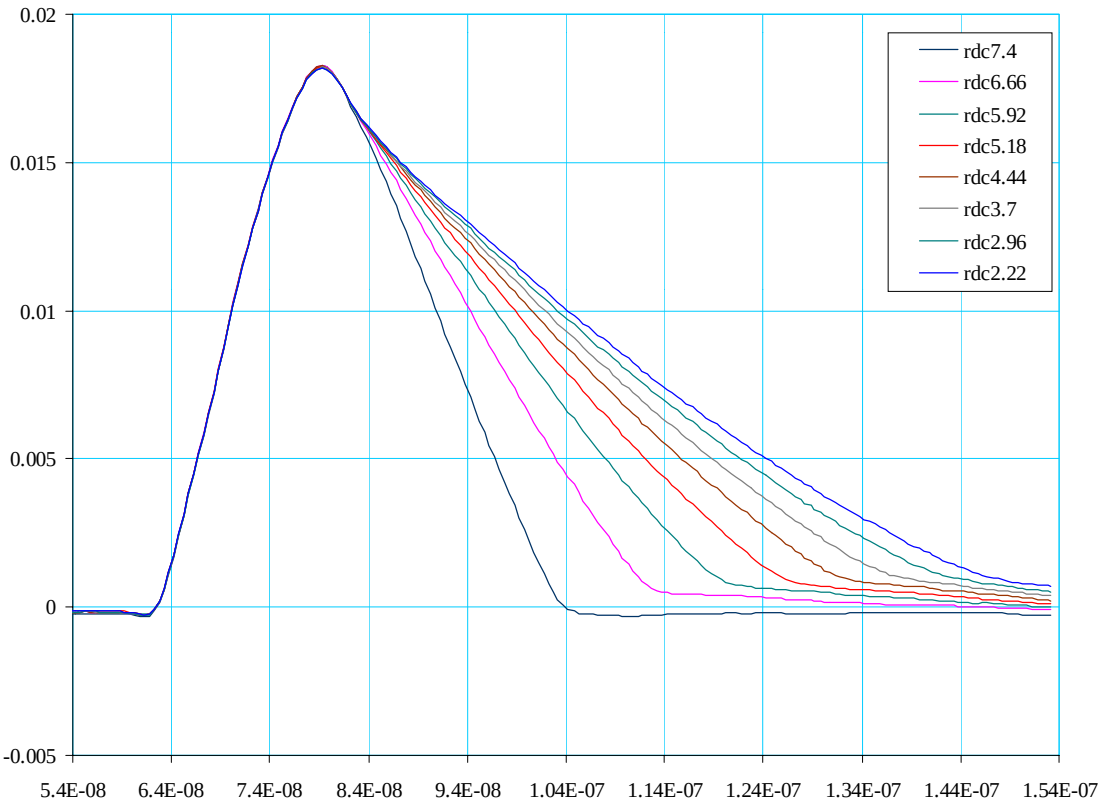


Scope traces of the Wilkinson capacitor voltage, charge-up and run-down, for all 16 integration gate widths. Note that for the longest gates, the capacitor starts to discharge already before the end of the charge-up phase (integration gate) because the pulse at the Wilkinson input has already crossed 0. Compare to the integrated shaper pulse of section 2.3 (see inset).

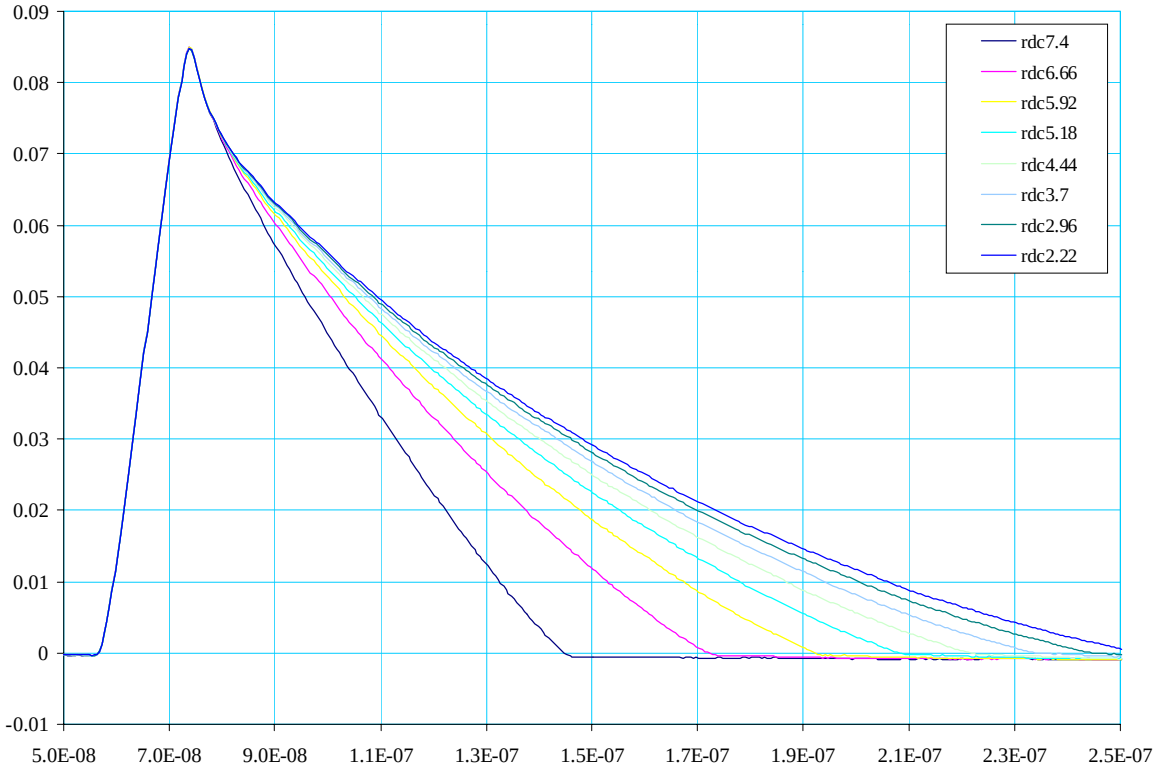
4.3 Rundown curren



Relation of Wilkinson output pulse width and rundown current for a mid-sized 400mV single into 50fF injection capacitor signal (40 fC). Parameters: Integration gate: 26ns, Threshold DISC1: 60mV (nominal), Threshold DISC2: 88mV, Hysteresis DISC1: 33 mV.

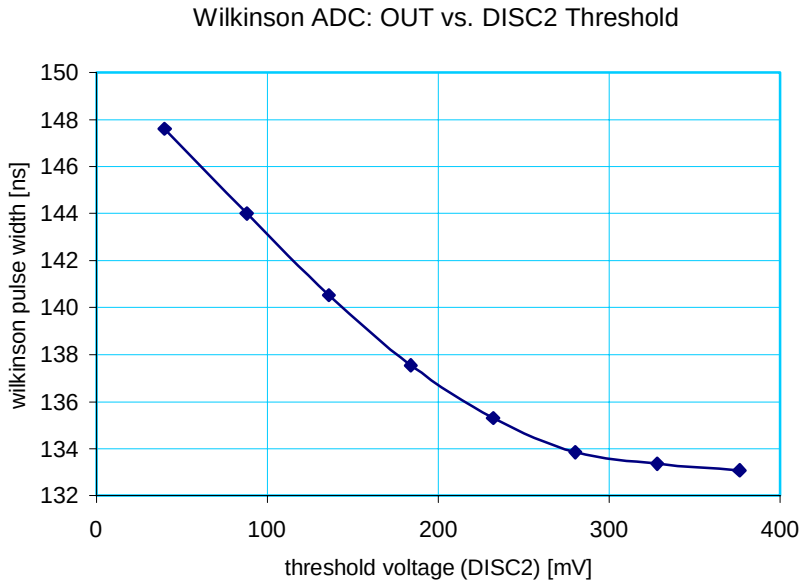


Scope traces of Wilkinson capacitor voltage, charge-up and run-down, for all 8 rundown current settings. The integration gate is close to nominal (~ 18 ns), the input signal is small.



Scope traces of Wilkinson capacitor voltage, charge-up and run-down, for all 8 rundown current settings. The integration gate is again close to nominal (~ 18 ns), the input signal is ~ 5 times bigger.

4.4 Threshold Disc2

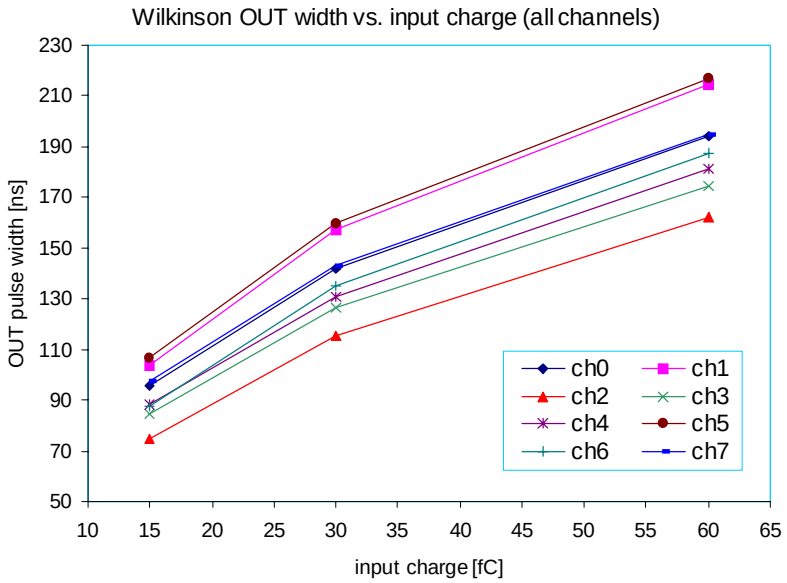


Influence of the Wilkinson discriminator (DISC2) threshold setting on the Wilkinson output pulse width.

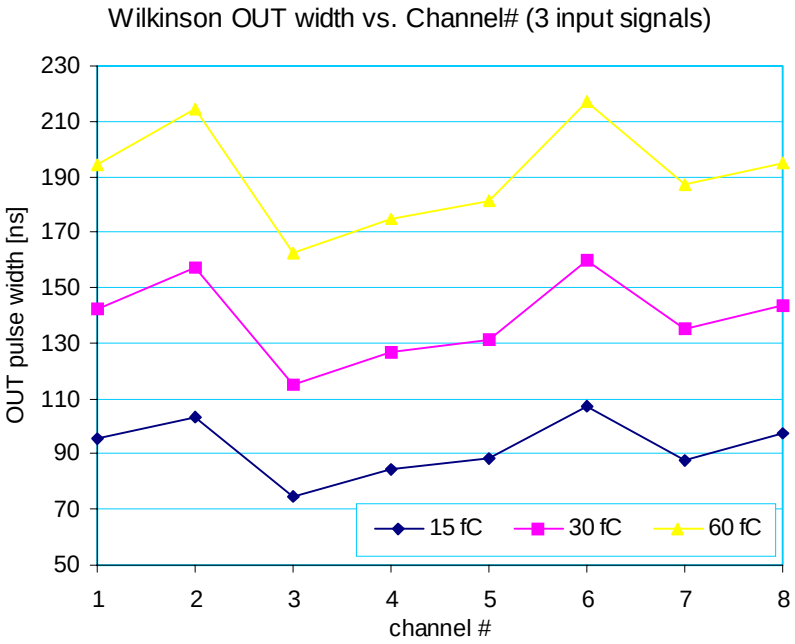
Parameters: Integration gate: 26ns, Threshold DISC1: 60mV (nominal), Hysteresis DISC1: 33 mV, Rundown current: 3.7 uA, Signal: 400 mV single into 50 fF (40 fC).

4.5 Output pulse statistics

A) Channel-channel variations



3 points on Wilkinson transfer curve (output pulse width vs. input charge) measured for identical signal and parameter settings on all channels of ASD01A-I.

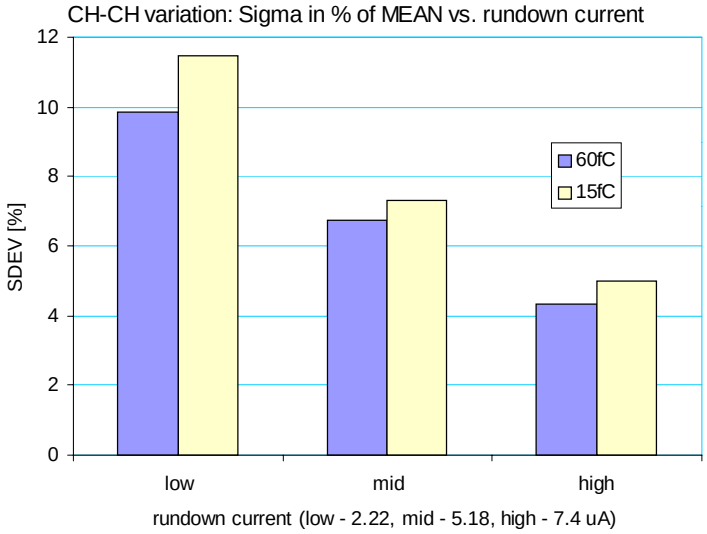


Wilkinson output pulse width for 3 input signals (15, 30, 60 fC) plotted across all channels.

Signal	15 fC	30 fC	60 fC
Mean	92.275	138.712	190.7
Stdev	10.592	15.09	18.756
Stdev%	11.479	10.878	9.835

Parameters (both plots): Integration gate: 16 ns, Rundown current: 2.22 uA Threshold Disc2: 88 mV, Threshold Disc1: 60 mV, Hysteresis Disc1: 33mV.

B) Channel-channel variations versus rundown current

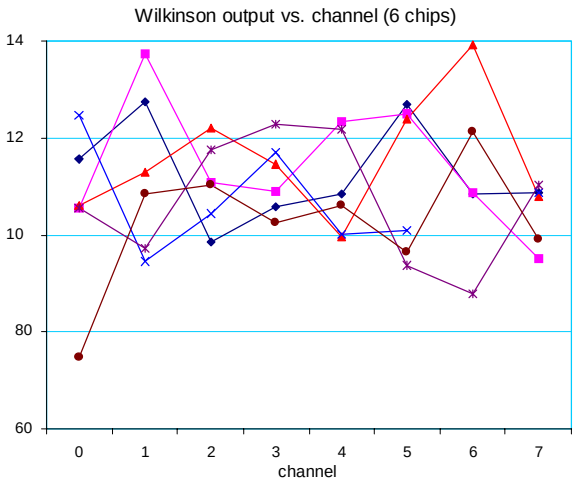


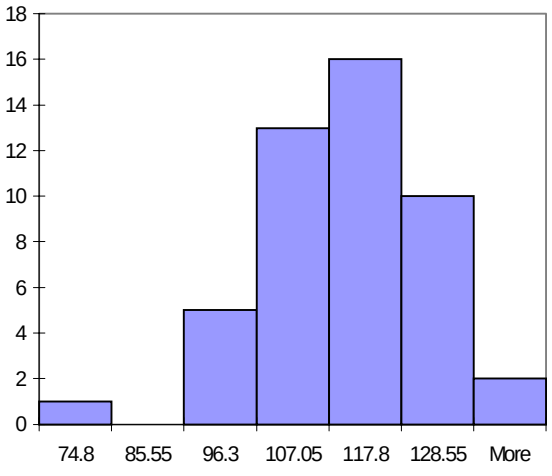
The rundown current influences ch-ch variations of the Wilkinson cell: The plot shows the sigma of the Wilkinson pulse widths of all channels for 2 signal charges and 3 different rundown current settings. The sigma (in percent of the mean pulse width across all channels) ranges from 4.3 % (larger signal, higher rundown current) to 11.5 % (smaller signal, smaller rundown current)

Rundown →	low		mid		high	
Signal	15	60	15	60	15	60
Mean	92.27	190.7	69.17	143.1	45.4	82.36
Stdev	10.59	18.75	5.06	9.636	2.270	3.553
Stdev%	11.48	9.835	7.315	6.733	5.000	4.314

C) Chip-Chip variation

Wilkinson output pulse width for one parameter set and one medium size input signal measured across all channels of 6 chips. (Parameters: VTH1: 80 mV, Gate: 15 nS, Shaper Out: 320 mV, I(Rundown): 3.7 uA).

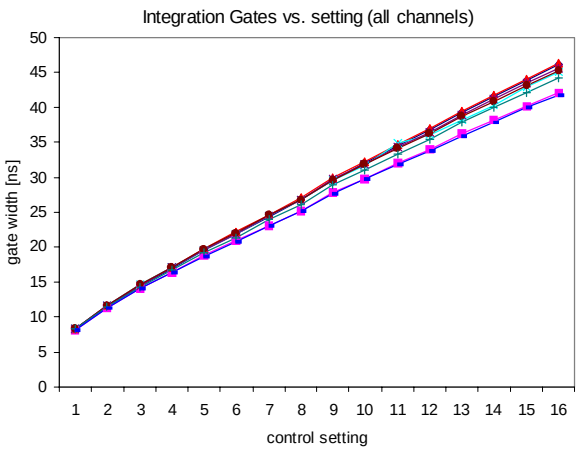


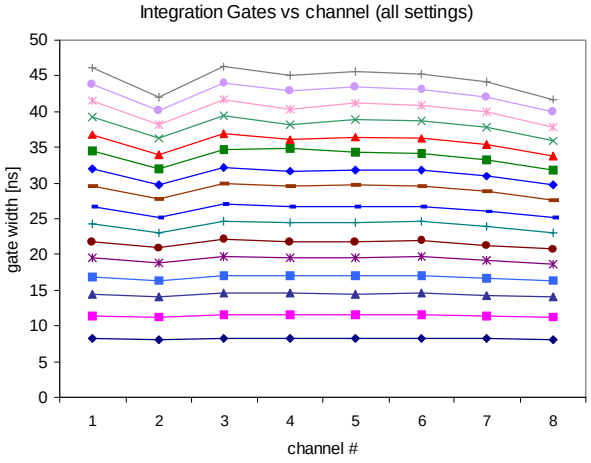


MEAN	109.94
SIGMA	12.46
SIGMA%	11.33%

4.6 Integration gate statistics

Integration gates measured on one chip across all channels for all settings.





Gate width	Sigma
15 ns (nom)	1.6%
45 ns (max)	3.9%

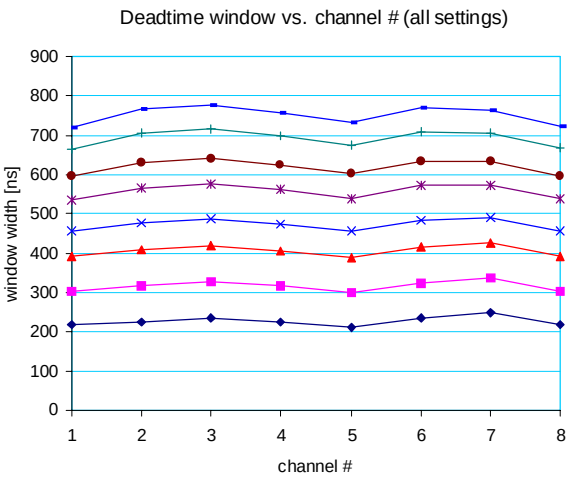
5. Deadtime

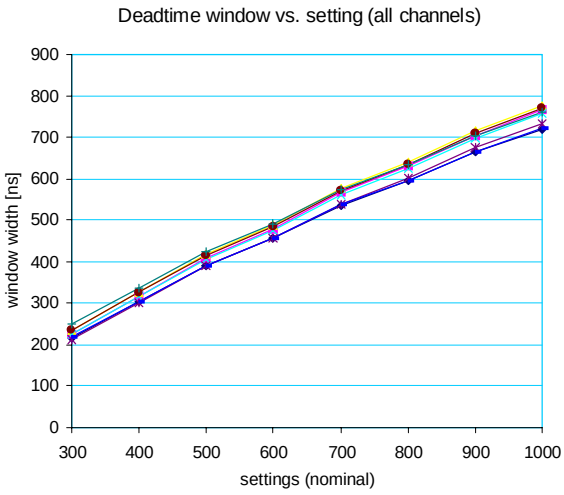
5.1 Window width and ch-ch statistics

Typical measurement of ASD01A deadtime window for all deadtime settings across all channels of one chip (ASD01A-III). The window width is the total deadtime, composed of the Wilkinson output pulse (charge-up plus rundown time of Wilkinson cap) and the added variable one-shot delay which is triggered by the falling edge of the output pulse. The linearity is satisfactory, the spread acceptable.

The maximum window mean width is about 25% below specification.

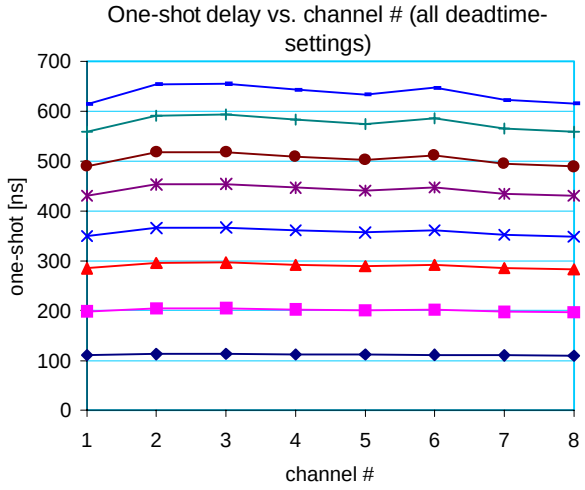
	0	1	2	3	4	5	6	7	MEAN	STDDEV	%
300	217	225.6	235.4	226.4	211.3	235.3	249.7	217.8	227.3125	11.658735	5.35%
400	304.6	317.4	327.3	317	300.3	325.4	336.9	304.5	316.675	12.046135	3.96%
500	390.7	408.5	418.5	406.5	388.8	415.5	424.7	390.7	405.4875	13.060478	3.34%
600	455.7	478.6	488.9	475.5	456.4	484.7	490.9	456.5	473.4	14.113557	3.09%
700	536.8	565.9	576.1	560.8	540.2	571.1	573.2	537.9	557.75	15.69355	2.92%
800	595.5	630.4	640.1	623.5	601.8	634.8	633.5	597	619.575	17.26541	2.89%
900	664.1	704.3	715.5	697.4	673.9	709.6	704.2	666.5	691.9375	19.194852	2.88%
1000	720.3	767.3	777.3	757.7	733.3	771	762	723.9	751.6	20.948091	2.89%

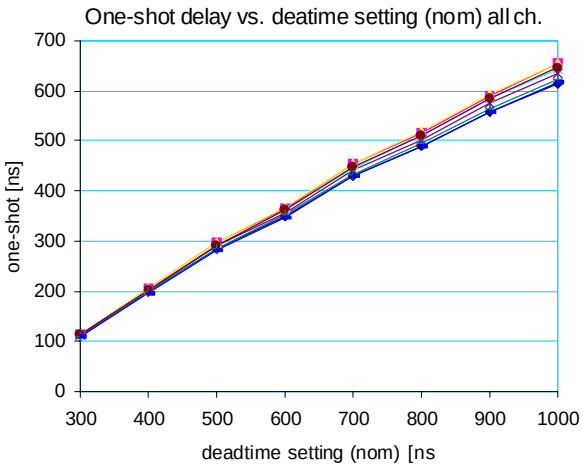


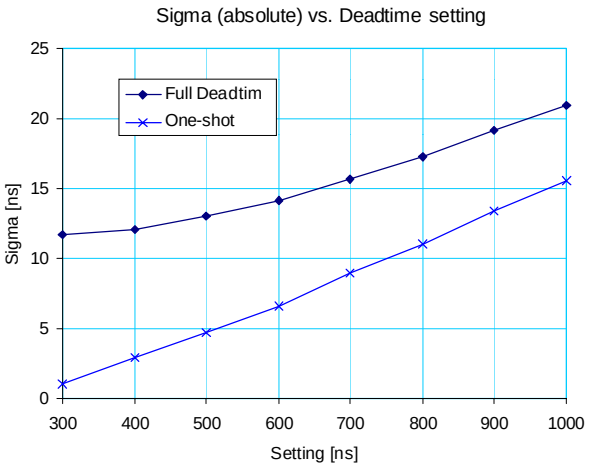


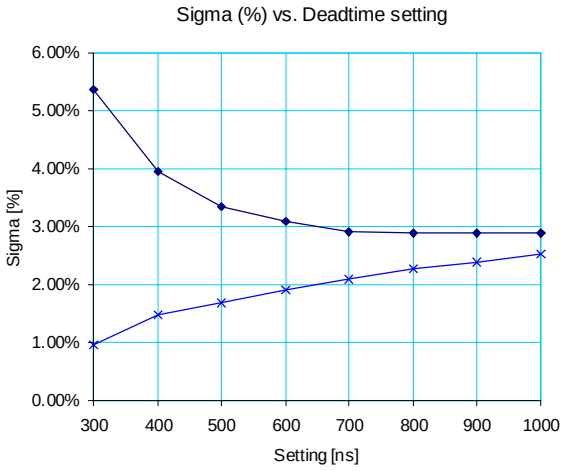
Subtracting the measured output pulse from the total deadtime yields the one-shot delay pulses:

	0	1	2	3	4	5	6	7	MEAN	STDDEV	%
300	111	112.6	113.2	111.9	111.8	111.4	110.4	109.8	111.5125	1.043357	0.009502
400	198.6	204.4	205.1	202.5	200.8	201.5	197.6	196.5	200.875	2.923076	0.014876
500	284.7	295.5	296.3	292	289.3	291.6	285.4	282.7	289.6875	4.726901	0.016721
600	349.7	365.6	366.7	361	356.9	360.8	351.6	348.5	357.6	6.617401	0.018988
700	430.8	452.9	453.9	446.3	440.7	447.2	433.9	429.9	441.95	8.979699	0.020888
800	489.5	517.4	517.9	509	502.3	510.9	494.2	489	503.775	11.0632	0.022624
900	558.1	591.3	593.3	582.9	574.4	585.7	564.9	558.5	576.1375	13.35739	0.023917
000	614.3	654.3	655.1	643.2	633.8	647.1	622.7	615.9	635.8	15.53649	0.025226







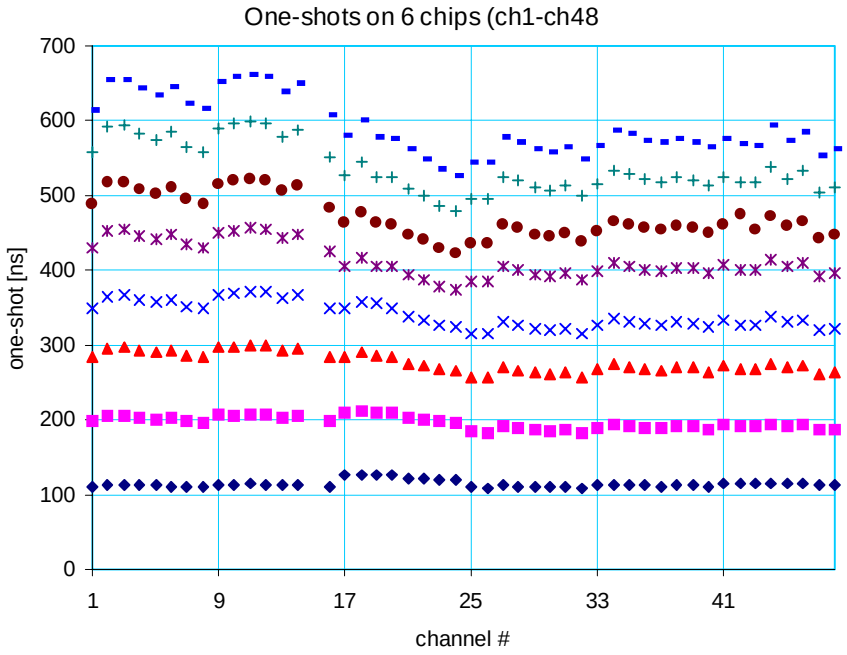


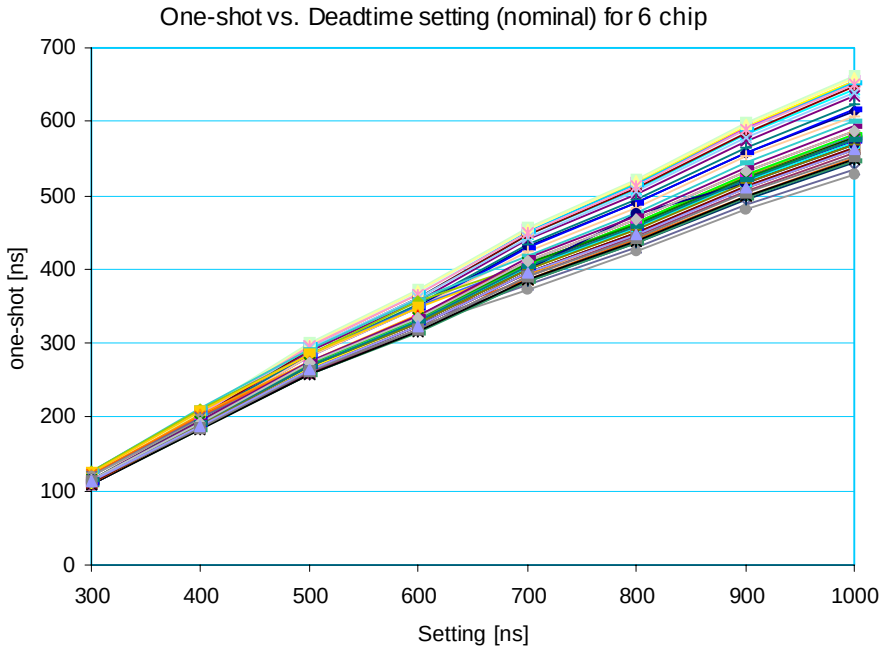
Sigma of the channel-channel variation on one chip (ASD01A-III) for the full deadtime window and the one-shot delay, absolute and in percent of the width.

Parameters used in all measurements: VTH1: 80 mV, Gate: 15 ns, Shaper Out: 320 mV, I(Rundown): 3.7 uA

5.2 Multi-chip statistics

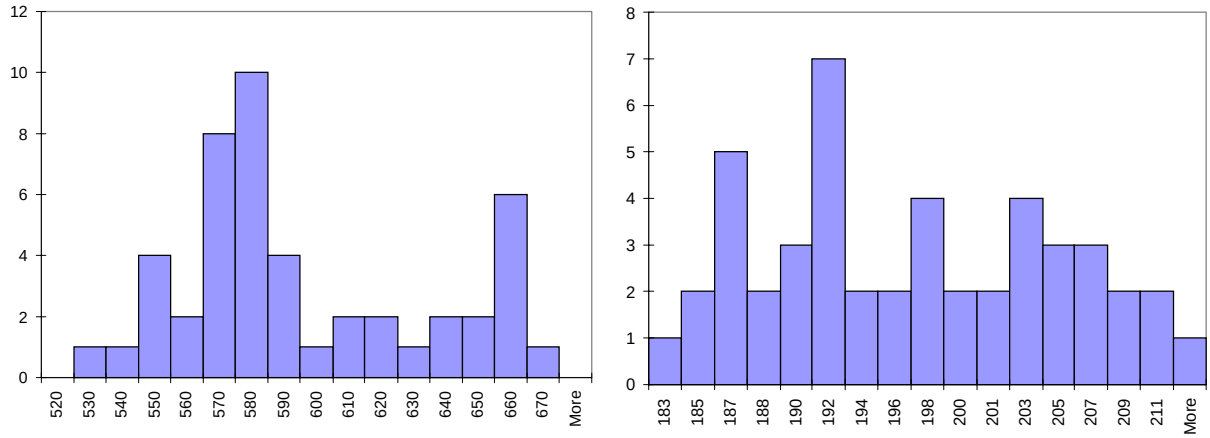
Measurement results on a total of 6 chips = 48 channels are available:



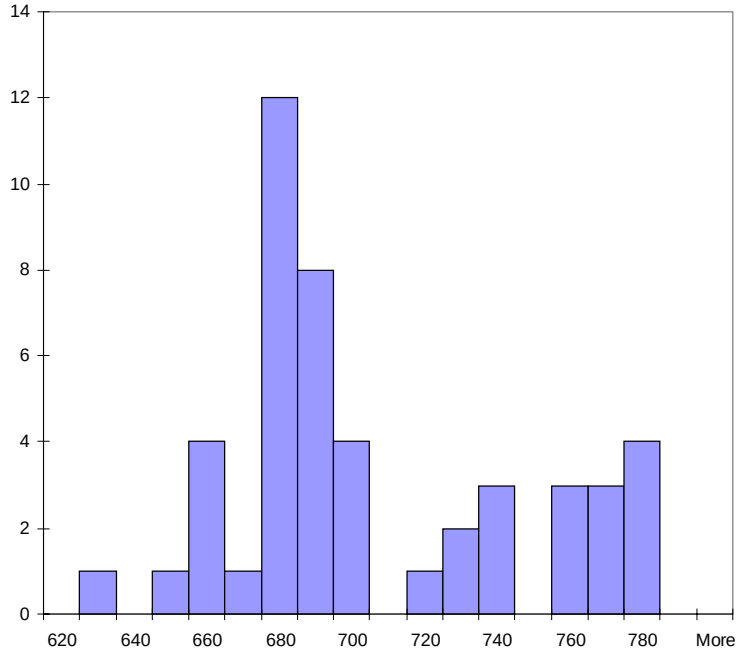


ONE-SHOT Statistics (48 channels/6 chips)

DT SETTING	MEAN	SIGMA	SIGMA%
300	113.9	4.72	4.14%
400	195.9	8.24	4.20%
500	276.6	13.0	4.70%
600	340.0	17.47	5.14%
700	413.1	23.73	5.74%
800	470.6	27.95	5.94%
900	536.3	33.56	6.26%
1000	591.0	38.01	6.43%



Histogramms of the one-shot delays of 48 channels - left: 1000 ns nominal deadtime setting; right: 400 ns nominal deadtime setting.

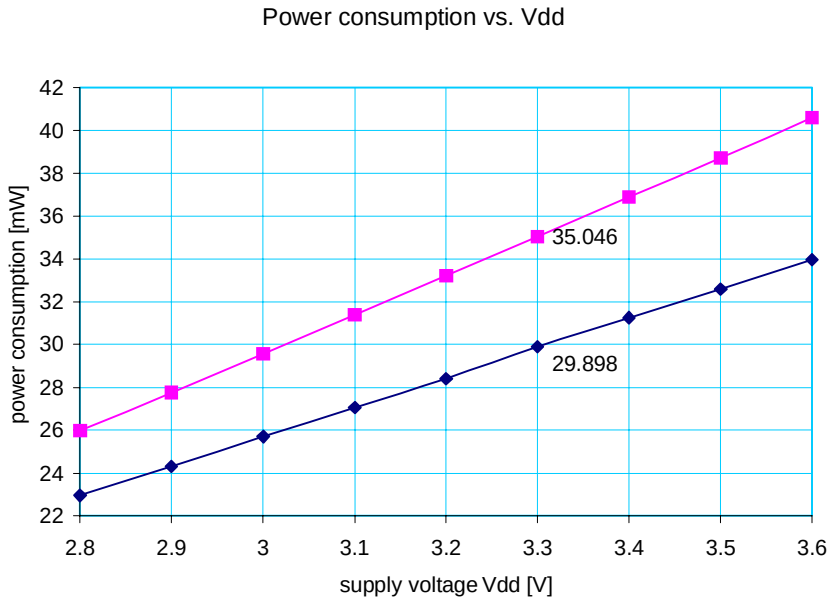


Histogramm of 48-channel full deadtime windows for typical parameter settings (VTH1: 80 mV, Gate: 15 ns, Shaper Out: 320 mV, I-rundown: 3.7 uA)

Statistical data:

MEAN	701.0
STDDEV	40.6
%	5.79%
MIN	622.3
MAX	777.3

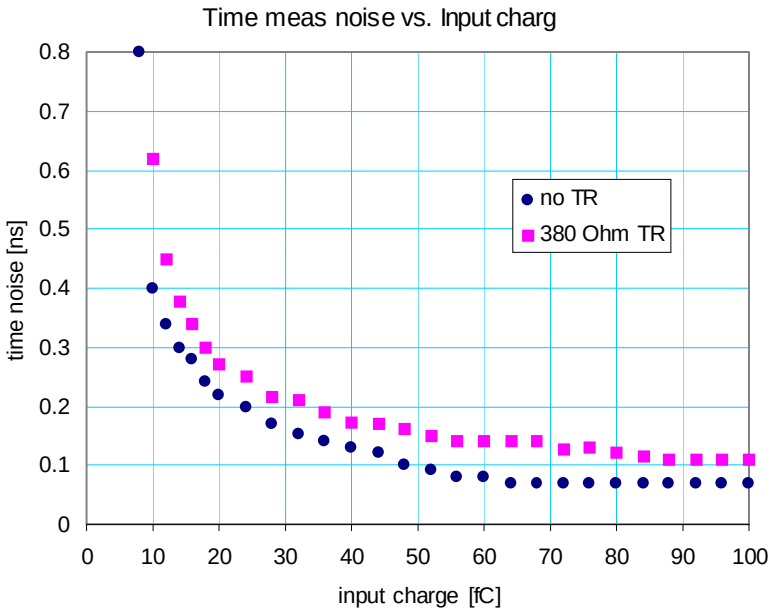
6. Power consumption



Power consumption measured with/without terminated LVDS drivers in mW per channel.

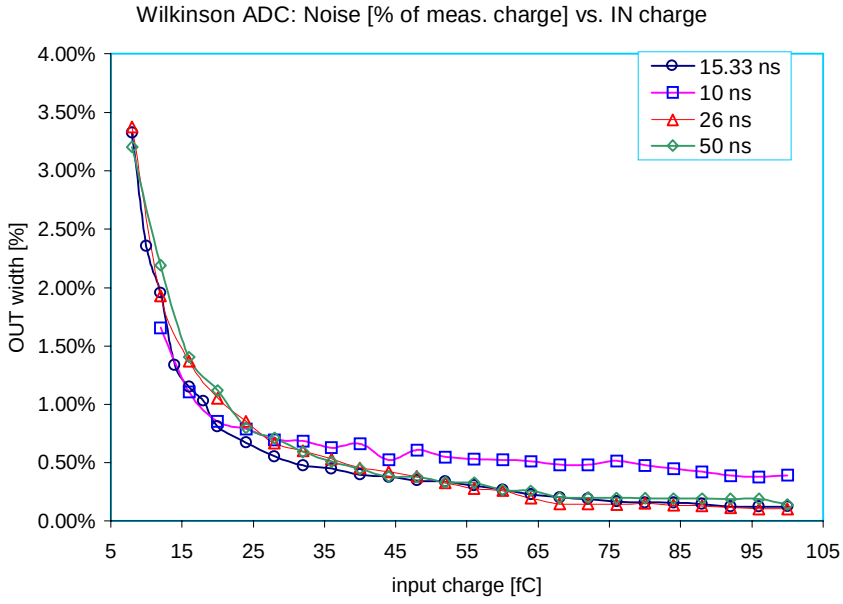
7. Noise performance

7.1 Time measuremen



Jitter of ASD output pulse leading edge as a function of signal strength at constant threshold (nominal, ~6fC). Bottom trace: floating pre-amp inputs; Top trace: with tube termination resistor (380 Ω).

7.2 Charge measurement



Jitter of Wilkinson pulse width as a function of signal strength at constant threshold (nominal, ~ 6 fC) for different integration gate widths (with tube termination resistor).