



# **Muon MDT Front End Electronics (WBS 1.5.9)**

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**DOE/NSF Review of U.S. ATLAS  
Detector**

**(with help from: E. Hazen, J. Oliver, C. Posch)**



# MDT Front End Electronics

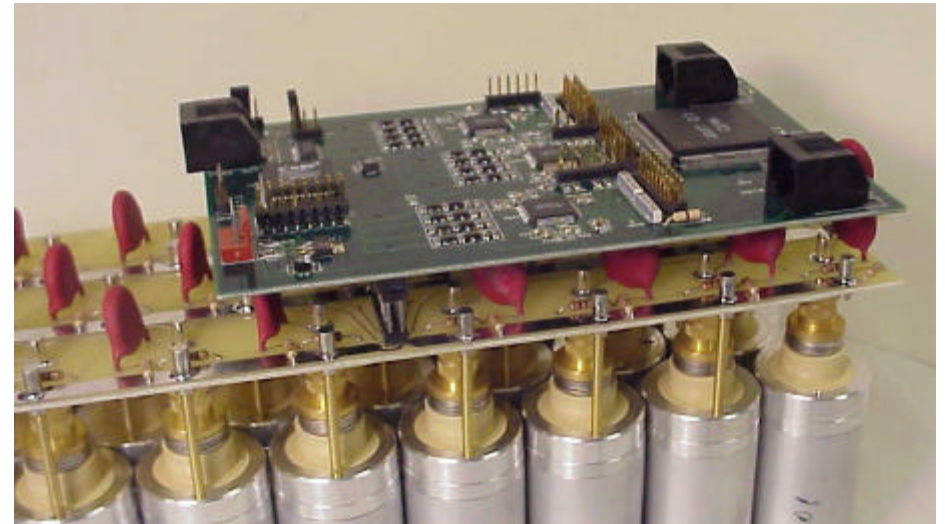
## Overview:

- The major deliverables:

- ◆ Amplifier/Shaper/Discriminator (ASD) Chip
- ◆ “Hedgehog” Boards
- ◆ “Mezzanine” Boards

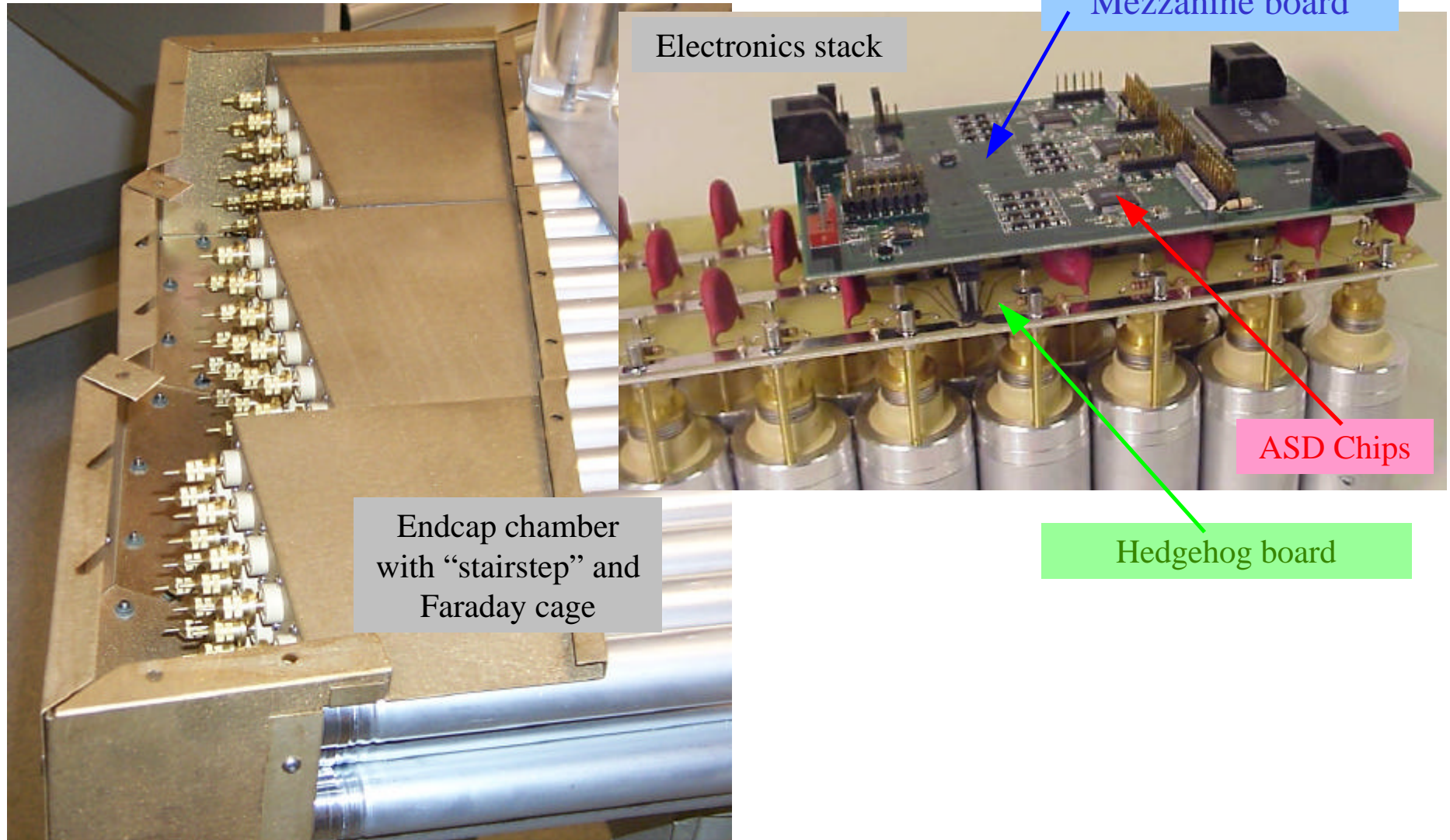
- Cost drivers

- Schedule issues





# The Major Components

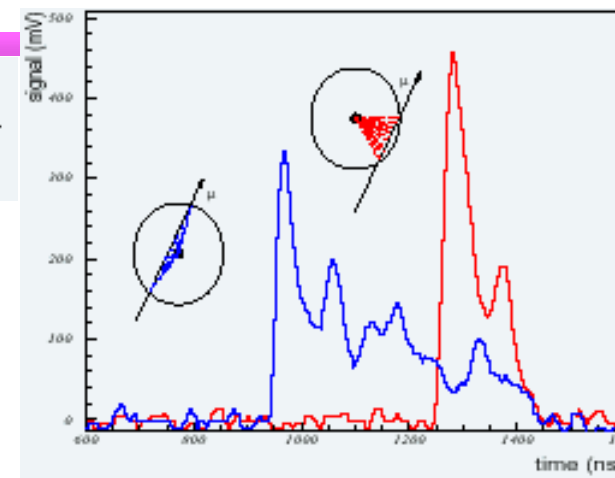




# MDT Operation Principles

## Proportional drift tube

- Position measured from drift time



## Mechanical Layout

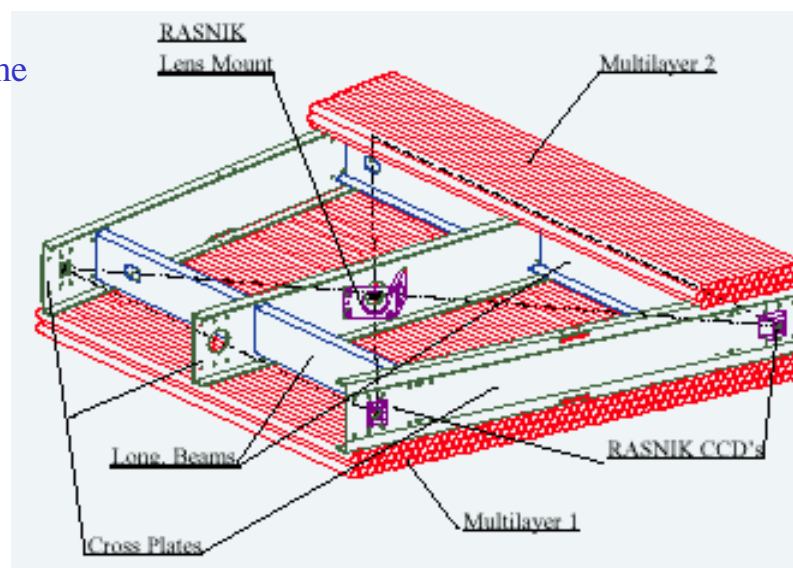
- 30 mm  $\varnothing$  Al tube 400  $\mu$ m thick wall
- 50  $\mu$ m  $\varnothing$  W-Re anode.
- Two 3 or 4 tube layers/chamber
- 1194 chambers
- 370,000 readout channels

## Operating Point

- Ar/CO<sub>2</sub> 93%/7% gas mixture
- 3 bar gas pressure
- $2 \times 10^4$  gas gain

## Performance:

- ~ 700 ns maximum drift time
- 80 mm resolution/tube

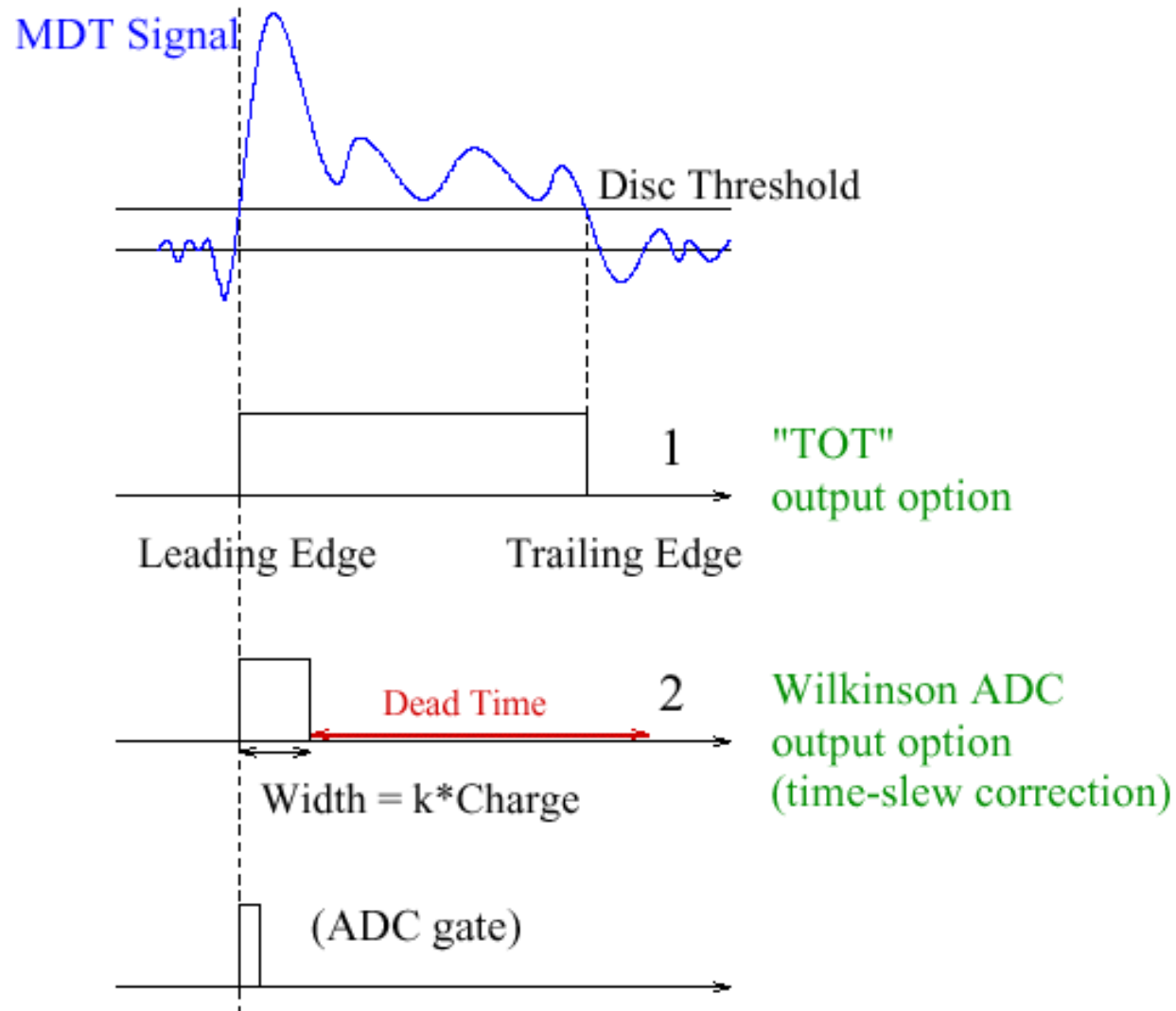


## Mechanical tolerance

- Wire/tube: 10 mm
- Wire/chamber: 20 mm
- 100 mm concentricity tubes-wire.
- Monitored with RASNIK system



# ASD Functionality





# Near-term deliverables

- **Electronics for chamber “Module 0”s**
  - ◆ **ASD lite**
    - ◆ 4 channel version with limited functionality
  - ◆ **Mezzanine lite**
    - ◆ CERN TDC (existing) + logic to control ASD lite
  - ◆ **Standard Hedgehog boards**
  - ◆ **10,000 channels being produced for 11 worldwide chamber construction sites.**



# ASD Lite

- **ASD Lite Features**
  - ◆ 4 channel complete Amp./Shaper/Discr.
  - ◆ Externally controlled threshold, hysteresis, bias
  - ◆ Linear output for 1 channel
- **Status**
  - ◆ Extensively tested on-chamber
  - ◆ 16k chips produced. 4400 packaged
  - ◆ Semi-automatic testing completed (**yield 95%**)
- **Remaining:**
  - ◆ Assemble and test on Mezzanine boards.



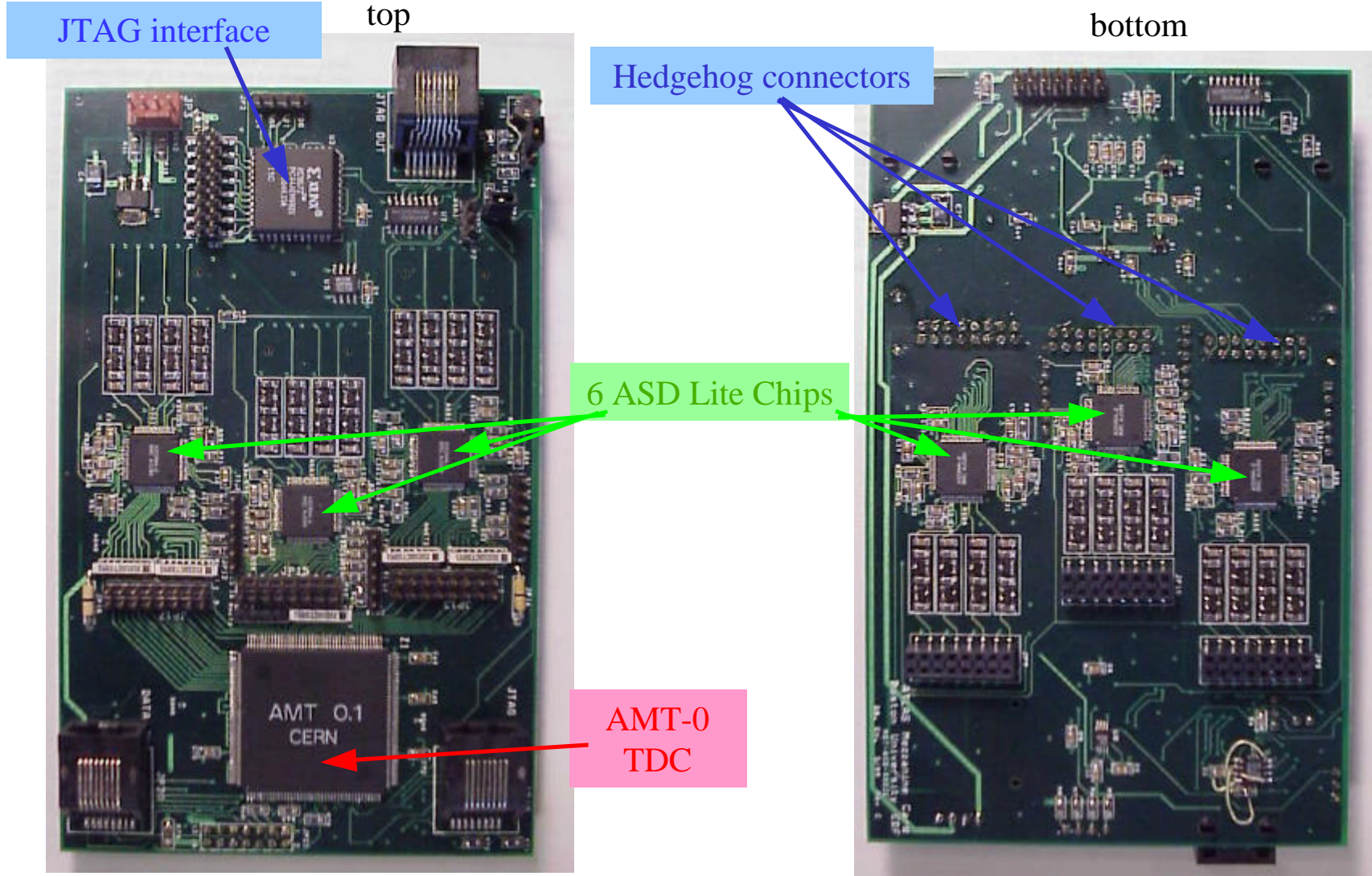
# Mezzanine Lite

- **24 Channel board with TDC**
- **JTAG Programming of Thresholds**
- **Mezz. Board is plug-compatible with final TDC**
- **10 boards produced and tested**
- **Full system test with CSM-0 (custom VME board for TDC readout) starting mid-March**
- **Components ordered, minor board layout changes being finalized**





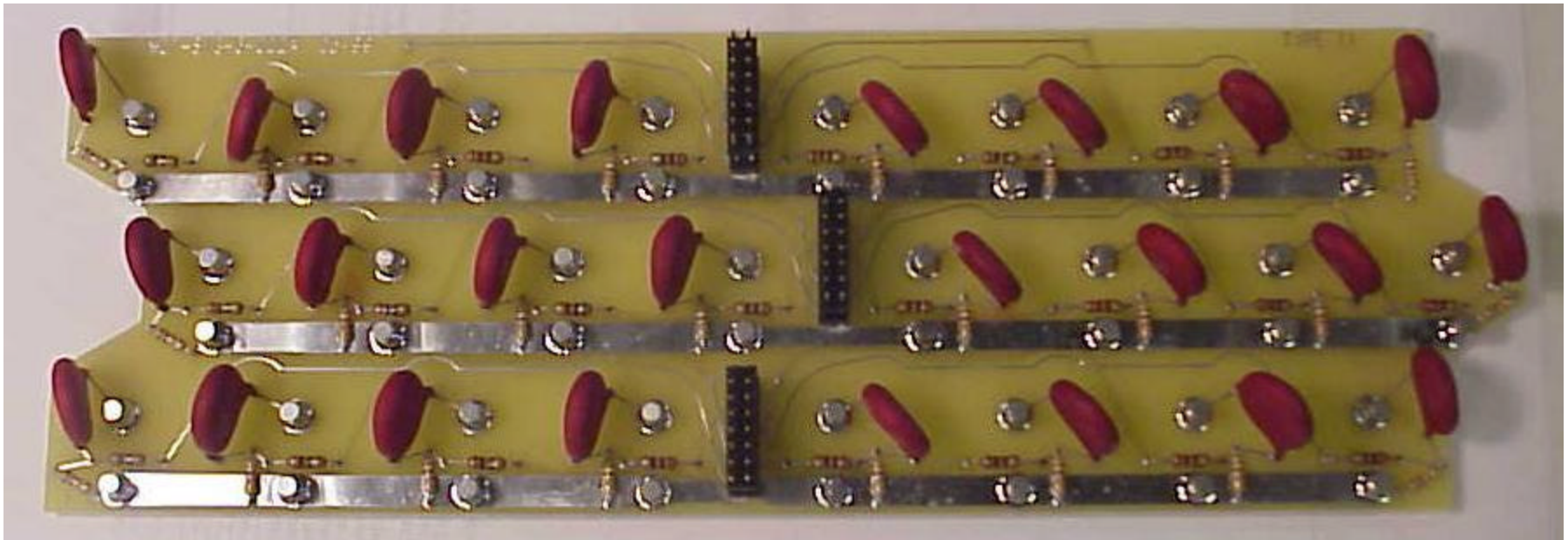
# Mezzanine Lite





# Hedgehog Boards

- 24 Channel board mounts directly on tubes. Blocks HV, carries signal to Mezzanine board
- Prototypes tested by various collaborators
  - ◆ First production of 100 boards completed
- 300 needed for chamber Module 0's





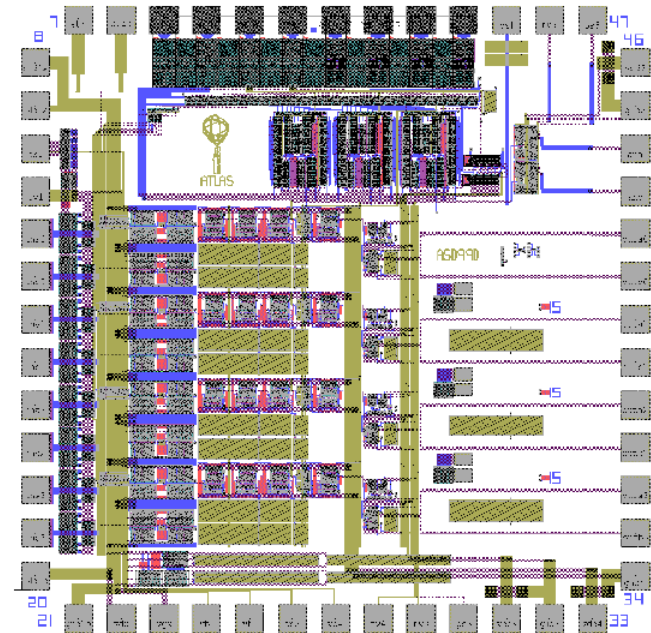
# Production ASD Chip-History

- ◆ **1996: Integrated 1.2  $\mu\text{m}$  CMOS Preamp+Disc prototyped**
- ◆ **1997: Changed to HP 0.5  $\mu\text{m}$  process ASD+LVDS**
  - ◆ Confirmed specs in new process, evaluated LVDS outputs
- ◆ **1998: Develop ASD lite full 4-channel chip**
  - ◆ Reduced crosstalk from 5% to 0.3% (unmeasurable)
  - ◆ Demonstrated stable operation on chamber, met all specs
  - ◆ Changed baseline design for new gas mixture (bipolar shaping)
- ◆ **1999: Package+test 4400 ASD lites, prototype ADC, logic**
  - ◆ Demonstrated high yield (95%). Tight parameter control in production
  - ◆ Built and tested Wilkinson ADC on chamber
  - ◆ Developed and submitted programmable ASD lite
- ◆ **2000: Beam test validation of analog path, first Octal ASD**
  - ◆ Submit, test bipolar shaping
  - ◆ Test programmable ASD lite
  - ◆ Full, programmable Octal prototype development underway (Posch)
- ◆ **2001: Second Octal prototype (production prototype)**
- ◆ **2002: Finish ASD Production**



# Production ASD Chip

- On going ASD development work:
  - ◆ Wilkinson ADC
  - ◆ Bipolar shaping
  - ◆ Programmable Control and Charge injection
  - ◆ 8 channels/chip





# ASD Programmable features

## 1) Test pulse injection

3-bit capacitor select	10 fC – 80 fC (8 switched 50 fF - capacitors @ 200mV)	3
8-bit mask register	select channels for calibration injection	8

## 2) Discriminators

Location	Variable	DAC type	Res	LSB	Range	comments	
DISC1	<b>Threshold:</b> $V_{DD}/2 \pm 128\text{mV}$ complementary, > 4 times nominal threshold ( $\pm 30\text{mV}$ )	VDAC (R-chain)	8-bit	1 mV	256 mV	at last gain stage (DA4 input)	8
	<b>Hysteresis:</b> 0 – 20mV (0 – 7 prim. Electrons), @ threshold coupling	CDAC	4-bit	1.875 uA	300 uA	0 – 100mV hysteresis at DISC1	4
DISC2	<b>Threshold:</b> 0 – 128 mV	VDAC (R-chain)	4-bit	16 mV	128 mV		4
	<b>Hysteresis:</b> fixed						

## 3) Wilkinson ADC

Variable	Nominal, adjustable range	DAC type	Res	LSB	range	
"run down"-current	$T_{NOM} = 70\text{ ns}, 35\text{ ns} - 140\text{ ns}$	CDAC	4-bit	1 uA	16 uA	4
gate (time window) width	$T_{NOM} = 15\text{ ns}, 8\text{ ns} - 64\text{ ns}$	-	5-bit	-	-	5
dead time	$T_{NOM} = 10 - 20\text{ ns}, 0 - 1024\text{ ns}$	-	4-bit	-	-	4

## 4) DC Offset (most probably eliminated in bipolar version)

Variable	adjustable range	DAC type	Res	LSB	range	
DC level after 1. shaper/gain stage	few 100 mV	2 x CDAC	4-bit	-	16 uA	8

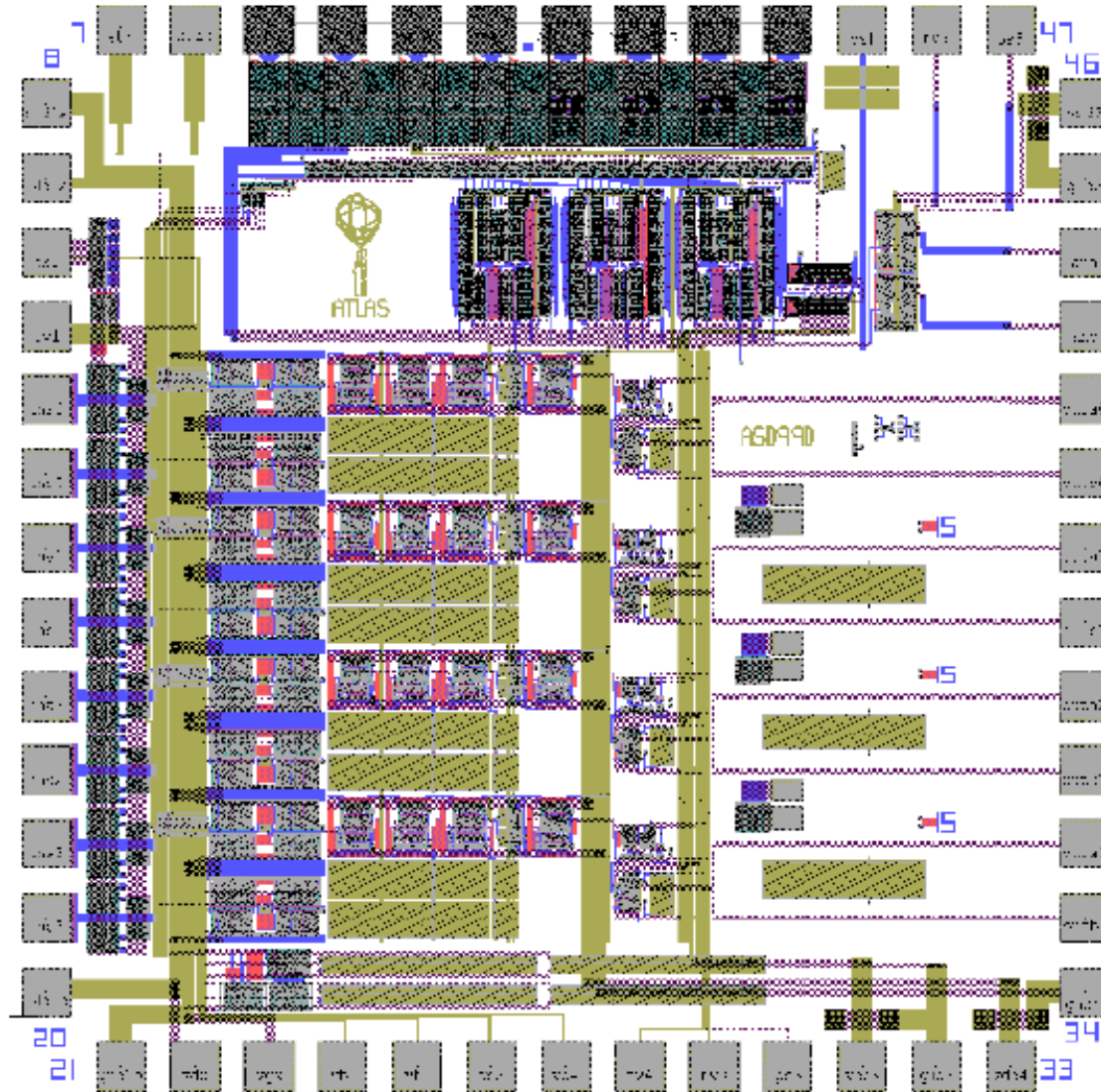
## 5) Output

Channel mode	HI, LO, Active, Disable (GND) preamp	2-bit / channel	16
Chip mode	TOT (Time Over Threshold), ADC	1-bit	1

**Total bits: 57 (63)**



# 4 Channel ASD Layout

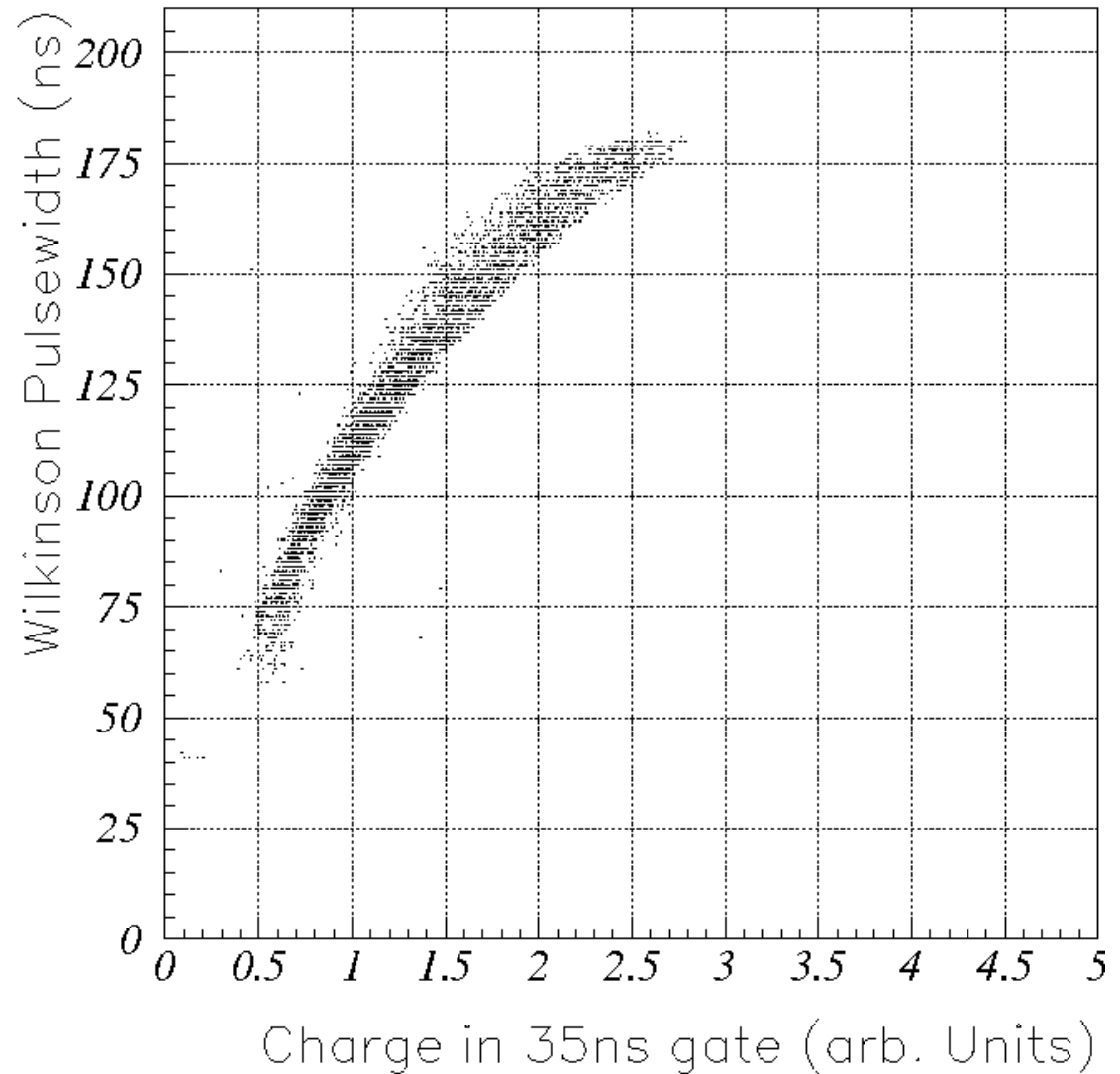




# ASD Lite Recent Measurements

Tests of the Wilkinson ADC  
(conventional capacitor run-  
down technique)

Tests performed on a prototype  
chamber with Am source.

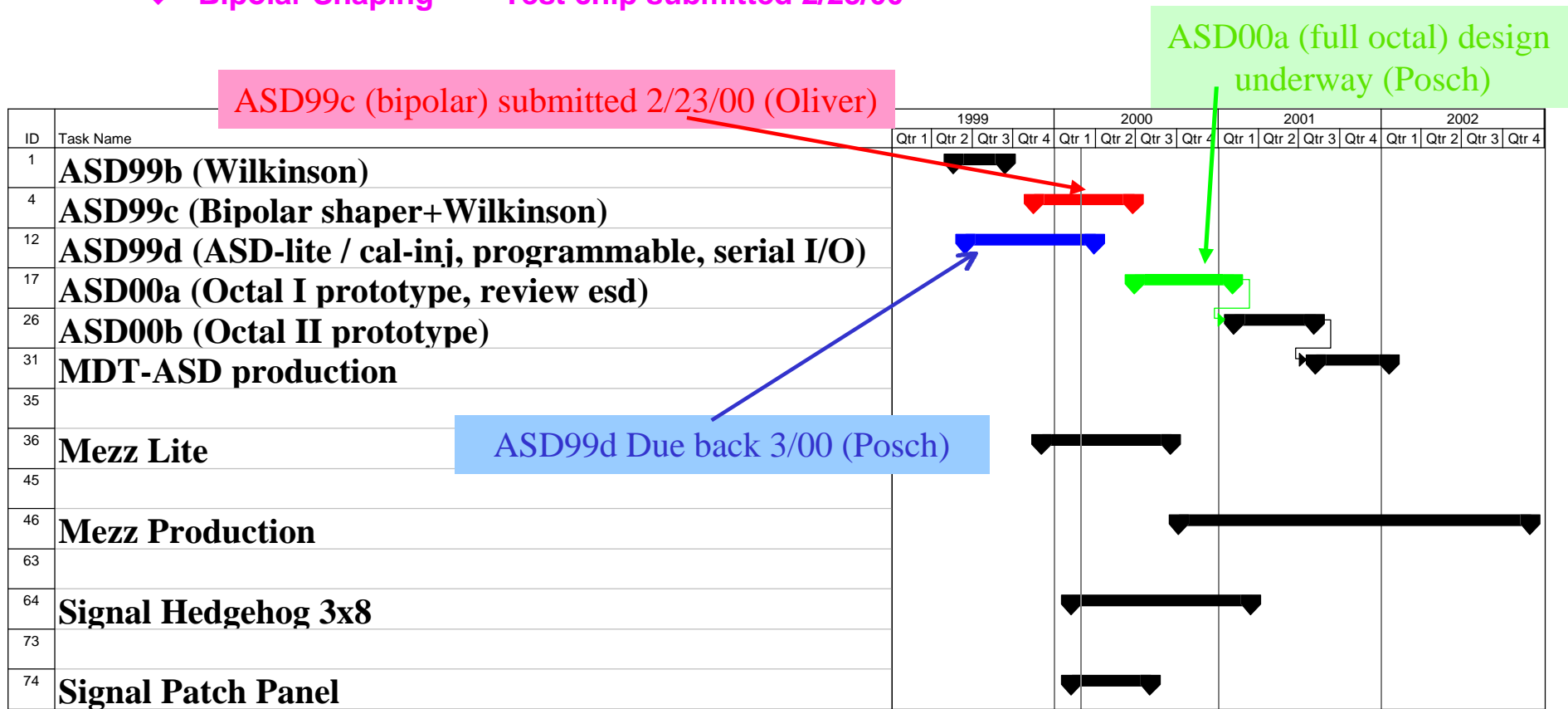




# Production ASD Status

- Production Schedule**

- ◆ Wilkinson ADC for Time Walk Correction    Tested Summer 99
- ◆ Complete programmability/charge injection    Test chip due 3/00
- ◆ Bipolar Shaping    Test chip submitted 2/23/00







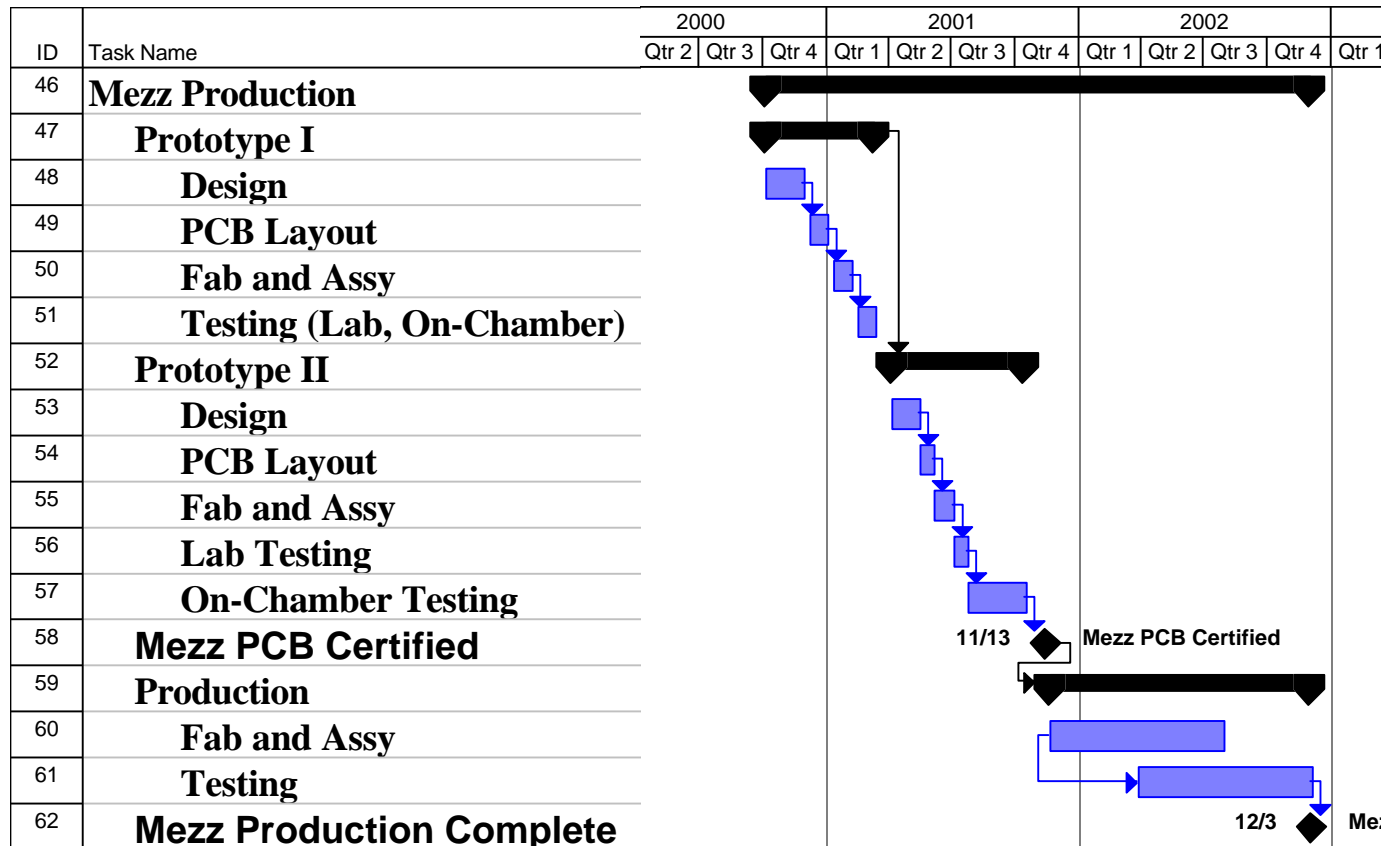
# Cost Drivers

- **Total ETC 1.5.9 ~ \$3.7 M**
  - ◆ **Mezzanine cards (Qty. 15,479)**
    - ◆ **\$117. Each \$1.9M**
      - 4 layer board
  - ◆ **ASD (Qty. 65,824)**
    - ◆ **\$780k**
      - Most engineering already complete
  - ◆ **Hedgehog boards (Qty. 4400)**
    - ◆ **\$103. Each \$460k**
      - Expensive HV coating



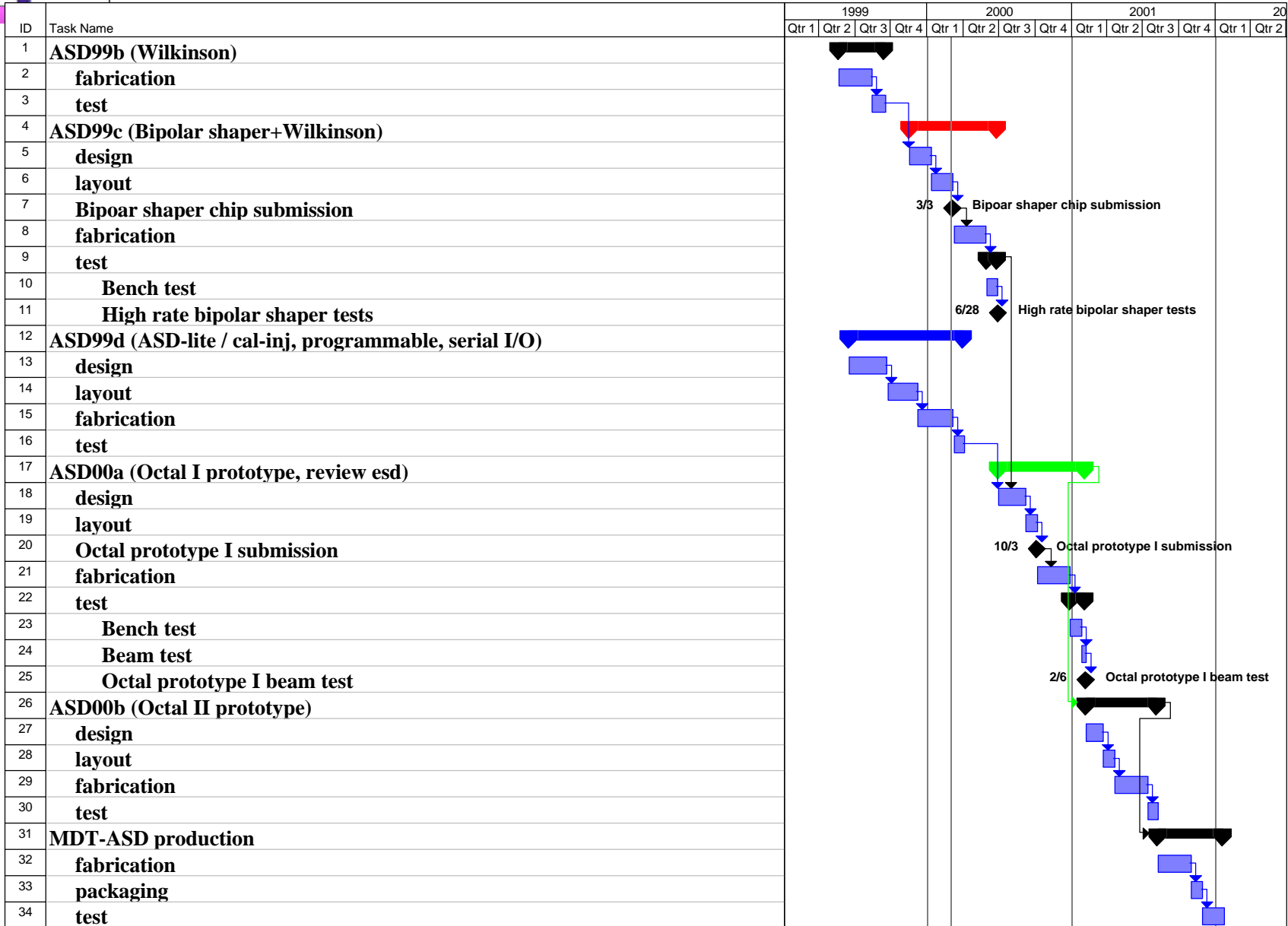
# Critical Path Items

- ASD development/production
- Mezzanine board production/testing





# Critical Path Items: ASD





# Summary

- **Most design issues solved.**
- **Schedule slipped ~9 months from baseline**
  - ◆ **Not too bad a match with world-wide chamber construction.**
- **Very close to original 1997 budget**