ATLAS Internal Document
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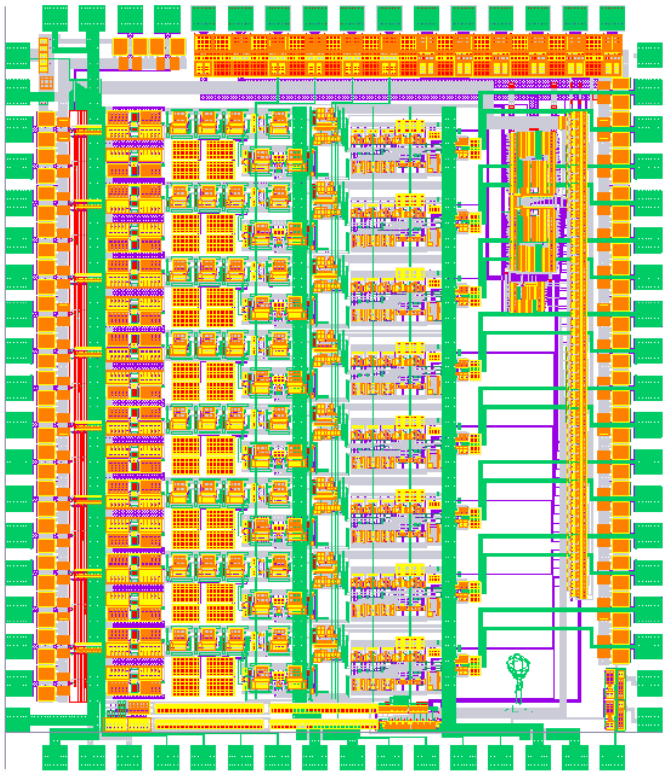
ATLAS Muon Spectrometer
MDT - Monitored Drift Tubes

ASD Amplifier-Shaper-Discriminator



Preliminary Design Review Report

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1 Introduction

1.1 MDT system overview

1.1.1 General

The ATLAS MDT system consists of about 350,000 pressurized drift tubes of 3 cm diameter, with lengths from 1.5 to 6 m. The MDTs are read out by an ASD at one end, and the other end is terminated with the characteristic impedance of the tube (370 Ω). The pre-amp input impedance is a relatively low (~ 100 Ω) to maximize collected charge. To minimize cost, the MDT signals are carried on two-layer "hedgehog boards" to a mezzanine board, which contains 24 readout channels: 3 Octal ASDs, a single 24-channel TDC, and associated control circuitry. A single MDT chamber may have as many as 432 drift tubes or 18 hedgehog/mezzanine board sets. Data are read out of each TDC individually via a 40 Mbit/sec serial link to a single CSM (Chamber Service Module) which multiplexes the (up to) 18 serial links into a single optical fiber for transmission to the ATLAS DAQ. A daisy-chain JTAG bus permits downloading of parameters to ASDs and TDCs and triggering of test/calibration pulse injection. Each superlayer (3 or 4 layers of individual tubes) is entirely enclosed in a faraday cage shield at both ends. All AC signals entering or leaving the shield are low-level differential signals (LVDS). All DC signals are filtered at the shield entry point. Each complete MDT chamber is electrically isolated from the support structure, and all services (gas, electrical, etc) are also electrically isolated or floating at the source. The MDT chambers will be individually grounded in a controlled way to a single common ground point.

1.1.2 MDT chamber properties

Some properties relevant for the design of the readout electronics of the muon drift tubes are summarized in Table 1.

Table 1. MDT properties

Length	≤ 6 m
Diameter	30 mm
Wire diameter	50 μm
Wire resistance	44 Ω / m
Impedance (Z_0)	380 Ω
Termination	380 Ω in series with 470 pF
AC coupling capacitor	470 pF
Drift gas	Ar/CO_2 (93%/7%)
Maximum background rate	400kHz

1.1.3 Drift gas issues

The drift gas Ar/CO_2 93/7 was chosen in large part because of its favourable ageing properties in the LHC environment. It is, however, a non-linear drift gas and this results in some difficulties for the ASD design. In particular, the non-linear r-t relationship results in a significant probability of late arriving clusters. This has been simulated extensively [7], [8], [9], and results in significant after-pulsing of the resulting signal. We expect approximately three output pulses for each muon track and this can result in difficulties for track reconstruction. It has been shown, again by extensive simulation [7], [8], [9], that introducing dead time for entire drift time of the MTD substantially eliminates this problem while minimally impacting track reconstruction efficiency. Thus, programmable deadtime, up to 1 μs, is a requirement of the design.

1.1.4 On-chamber readout electronics

The ASD chips are mounted on a “mezzanine” card which is in turn connected to a chamber mounted “hedgehog” card. Each mezzanine card contains three MDT-ASD for a total of 24 channels per mezzanine-hedgehog combination. The hedgehog contains no active circuitry and is fully contained within a faraday cage.

1.2 Front End Requirements

The ATLAS Muon Spectrometer aims for a P_T resolution of 10% for 1 TeV muons. This translates into a single wire resolution requirement of < 80 μm. The average drift velocity is about 20 μm/ns, which implies a systematic timing error for an individual tube of about 500 ps. The planned gas gain is low, about 2×10^4, to avoid aging problems. The expected signal (collected charge) is roughly 1500 electrons (0.25 fC) per primary electron, so good position resolution requires a low noise front-end. A specified pre-amp peaking time of 15 ns is a good compromise in terms of resolution and stability. The channel to channel crosstalk is specified to be less than 1%. The high count rates of up to 400 kHz/wire together with the long electron drift times require either a bipolar shaping scheme or active baseline restoration to avoid resolution deterioration due to baseline fluctuations. At the time of the TDR, the baseline MDT gas was $Ar/N_2/CH_4$ 91/4/5 (3 bars absolute) which is very linear and has a maximum drift time of 500 ns. The choice for the ASD shaping scheme was unipolar shaping with active baseline restoration for the following two reasons. First, it allows the measurement of the signal trailing edge, which has a fixed latency with respect to the bunch crossing, with an accuracy of about 20 ns. Second, it avoids multiple threshold crossings per muon track, which would increase the hit rate and therefore the readout occupancy. Aging problems with all MDT gases containing hydrocarbons caused a change of the baseline gas to Ar/CO_2 93/7 (3 bars absolute) which has a maximum drift time of 800 ns and is very non-linear. The long drift time and the non-linearity degrade the trailing edge resolution to about 80 ns and cause multiple threshold crossings even for a unipolar shaping scheme. We therefore have adopted a bipolar shaping scheme since it does not require an active BLR and also does not require programmable filter time constants. To avoid multiple hits from multiple threshold crossings for a single signal we introduce a fixed dead time equal to the maximum drift time. It was shown that the overall increase in dead time does not cause a degradation of the pattern recognition efficiency. An ADC will measure the signal charge in a given time window (integration gate) following the threshold crossing time. The charge is then encoded into a pulse width in the usual Wilkinson technique. This information allows a resolution improvement by performing a time slewing correction. Additionally, it is useful for diagnostics and monitoring purposes and might also be used for dE/dx identification of slow moving heavy particles like heavy muon SUSY partners. Two modes of operation will be provided. In one mode the ASD output gives the time over threshold information, i.e. signal leading and trailing edge timing. The other mode measures leading edge time and charge and is considered the default operating mode.

2 Design

The MDT-ASD is an octal CMOS Amplifier/Shaper/Discriminator which has been optimized for the ATLAS MDT chambers. The length of these chambers, up to six meters, requires the use of a terminating resistor to avoid confusion and pulse distortion from reflections. The noise contribution from this terminating resistor has been analyzed in detail and has been shown to be the dominant noise source in either a bipolar or CMOS ASD implementation [4], [2]. For reasons of cost and design flexibility, a high quality analog CMOS process has been chosen for this device.

2.1 Overview and specifications

The structure of each analog channel of the ASD is shown in Figure 1. It is a fully differential structure with a pair of identical preamplifiers at the input, a shaper stage, followed by a discriminator leading edge charge integrator to be described later. The second pre-amp provides DC balance, common mode pickup rejection and improved power supply rejection. The most relevant analog specifications include:

Table 2. ASD analog specifications

Input impedance	$Z_{IN} = 120\ \Omega$
Noise	ENC = 6000 e^- rms or ~ 4 primary electrons (pe^-)
Shaping function	bipolar
Shaper peaking time	$t_p = 15$ ns
Sensitivity at shaper output	3 mV/pe^- (gas gain 2×10^4) or 12 mV/fC (delta pulse into terminated MDT)
Linear range	1.5 V or 500 pe^-
Nominal threshold setting	60 mV or 20 pe^- (~ 6 σ_{noise})

2.2 Technology choice

2.2.1 Fabrication process

The fabrication process chosen for the MDT-ASD is a 0.5 μm n-well triple-metal CMOS process. There is a linear capacitor option consisting of polysilicon over an active N+ diffusion in an N-well. The process is silicided yielding very low polysilicon and diffusion resistivities. There is a "silicide" block layer available which allows exclusion of silicide over polysilicon but not over diffusion. This is used primarily for well behaved polysilicon resistors. The operating voltage is 3.3 V. The process parameters are apparently very tightly controlled and consistent run to run (Wafer Test Results and SPICE Model Parameters at [14]).

2.2.2 Process specifications

Table 3. HP 0.5μ CMOS process parameters

Parameter	n-channel	p-channel	either	Units
Minimum gate length			0.5	μm
Threshold voltage (typ)	0.76	0.88		V
Kprime	92	26		$\mu A/V^2$
N+ diffusion sheet resistance	2.2	2.2		Ω/sq
Poly sheet resistance (silicided)			2.0	Ω/sq
Poly sheet resistance (silicide blocked)			130	Ω/sq
Gate oxide thickness			100	Å
Gate capacitance			3.5	$fF/\mu m^2$
Linear capacitor			2.3	$fF/\mu m^2$
Vbkd	11.3	-9.6		V

2.3 Topology and architecture

The MDT-ASD utilizes the pseudo-differential input topology developed and implemented in many successful bipolar ASDs by University of Pennsylvania [6]. The overall topology is shown in the block diagram, Figure 1.

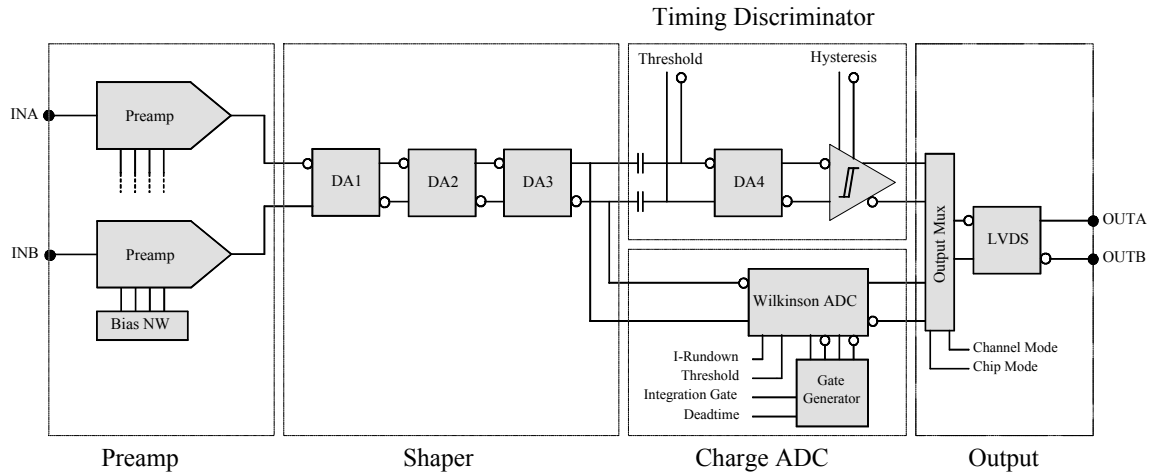


Figure 1. MDT-ASD channel block diagram

It is a fully differential structure from input to output for maximum stability and noise immunity. Each MDT connects to a "signal" pre-amp with an associated "dummy" pre-amp. This in turn connects to the mezzanine card but goes no further. It provides DC balance to the subsequent stages as well as some degree of common mode rejection from noise pickup, substrate coupling, and power supply noise. Following the pseudo-differential pair of pre-amps is a differential amplifier which provides gain and outputs a fully differential signal to subsequent stages. Following this are two stages of differential amplifiers which provide further gain while implementing bipolar shaping. Bipolar shaping was chosen to prevent baseline shift at the anticipated high level of background hits [7], [8], [9].

The shaper output is fed into a discriminator and Wilkinson ADC section. The ADC integrates the shaped pulse for a given gate width and stores the charge on a holding capacitor which is then run down at a constant rate[1]. The ADC output width thus encodes the "leading edge" charge. These data are used for time slew correction to enhance timing resolution.

The Wilkinson ADC operates under the control of a Gate Generator which consists of all differential logic cells. It is thus highly immune to substrate coupling and can operate in real time without disturbing the analog signals. The final output is then sent to the LVDS cell and converted to external low level signals.

Each complete ASD channel draws approximately 10 mA from a 3.3 V supply, thus dissipating 33 mW per channel. The operation of the MDT-ASD sub-cells is described in detail in subsequent sections.

2.4 Analog signal chain

2.4.1 Pre-amplifier

Specifications

- Power dissipation: 3.3 mW per pre-amp (~ 1 mA @ 3.3 V)
- Z_{IN}: 120 ohms (DC & AC/dynamic)
- Input noise density: 1.3 nV/$\sqrt{Hz}$
- ENC (with 380 Ω termination): 6000 e^- rms

[1] Integration gate and rundown current are variable (see section 2.6.1.3)

Description

The pre-amp is an unfolded cascode shown in the schematic in Figure 2.

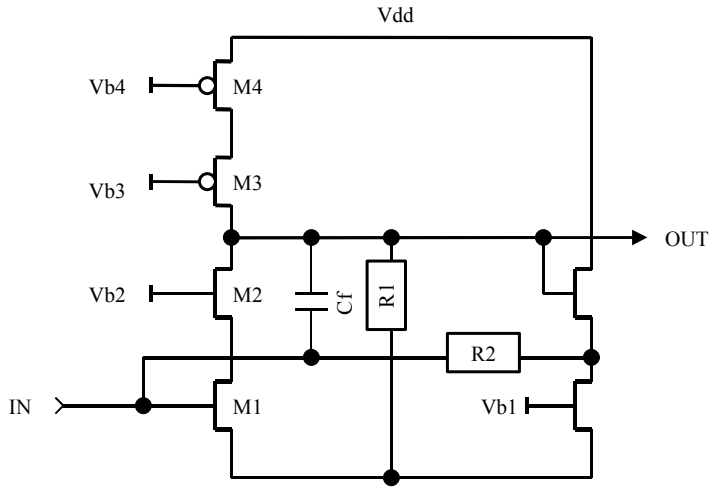


Figure 2. Pre-amp simplified schematic

The large input transistor M1 (2400 µm / 0.9 µm) operates at a nominal 1 mA standing current providing low noise and low input impedance at reasonable power dissipation. Transistor M2 constitutes the cascode. Current is supplied to the high impedance node via a cascode current source (M4 & M3). There is a 10 kΩ load resistor, R1, on the high impedance node which, along with feedback resistor R2 sets the low frequency part of the input impedance. The high frequency behavior of the circuit is determined by the feedback capacitor and the total parasitic capacitance on the high impedance node. This capacitance consists of the parallel combination of drain capacitances of M2 and M3, trace capacitance, and gate capacitance of the subsequent stages. Each of these is a well controlled process parameter with very low process variation. The value of feedback capacitor is chosen to produce uniform input impedance of 120 Ω across a wide range of frequency. Bias voltages V_b[1:4] are provided by a bias circuit (not shown) which is bypassed using large external capacitors.

2.4.2 Differential amplifiers

Each of the differential amplifies DA1 through DA4 is of the same basic design shown in Figure 3.

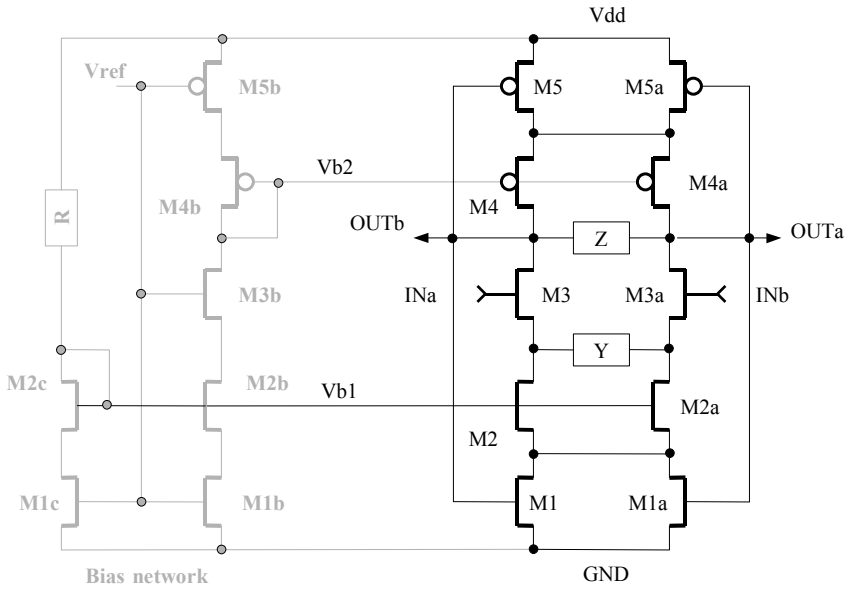


Figure 3. Differential amplifier schematic

The basic amplifier is a differential pair of transistors, M3 & M4, with gain set by load impedance, Z, and source impedance, Y. By tailoring these impedances with some combination of resistors and capacitors, one can obtain gain stages as well as more complicated pole/zero structures or bipolar shaping structures.

The DC operating point of the amplifier is established by common mode feedback. The output nodes, OUTB (OUTA) are connected to the gates of M1(1a) and M5(5a) respectively. These transistors operate in their linear region as resistors with, typically, 50 – 100 mV across them. Common mode gain is achieved by modulating these FET resistances via common mode output voltage. The gain of this loop is of order 10. Voltages VB1 and VB2 are set by the bias network shown to the left. Common mode feedback drives the common mode output voltage to V_{ref} which set to $V_{DD}/2$ or 1.65 V. Measured common mode output voltage is typically within 20 mV of this value. Total standing current in the circuit is set by the single polysilicon resistor, R.

Bandwidth of each of the differential amplifier stages is limited by load resistance and the total capacitance of the output node which consists of the parallel capacitance of output transistor drains, traces, and gate input of subsequent stage. Typically, each stage incurs a pole at a time constant of about 4 ns with an 11 kΩ load (~ 40 MHz 3dB – bandwidth per stage, see section 2.5.2)

Since gain of each diff-amp is largely determined by the ratio of load to source resistance (silicide blocked poly), the gain is desensitized to process variation.

2.4.3 Shaper

The shaper is composed of two stages of RC networks embedded in the differential amplifiers DA[2:3]. The first diff-amp DA2 implements a pole/zero network using a series parallel RC combination shown below in Figure 4. The values are chosen to cancel the very long time constant component of the positive ion MDT pulse. This shaping stage is, however not critical as the overall pulse shape is dominated by the following (bipolar) shaping stage.

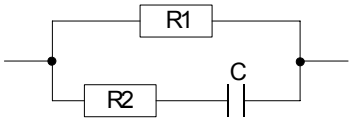


Figure 4. Pole/zero network

The second amplifier, DA3, uses a simple series RC network in its source location to effect a bipolar shaping stage. The RC product of this shaping stage is approximately 50 ns. The pulse thus formed by this stage achieves a high level of area balance within 10 shaping time constants or about 1/2 μs. This is short compared with the estimated average time between background pulses (2.5 μs or 400 kHz) and thus achieves good rejection to baseline shift.

2.4.4 Pre-discriminator gain stage

The shaper output is AC coupled to one additional differential amplifier, DA4, referred to as pre-discriminator gain stage which provides additional gain to the discriminator. This stage has smaller load resistance (5.5 kΩ) to provide lower driving impedance to the subsequent discriminator stage. Its source resistor is chosen to be zero to provide maximum gain and bandwidth at the expense of higher process variation of gain. Since the threshold is applied at its input however, the gain sensitivity to process variation is irrelevant.

2.4.5 Discriminator

The discriminator, shown below in Figure 5, is a high-gain differential amplifier with symmetrical current-mirror loads with main differential pair, M1/M2, biased at 400 μA. Two current-mirror “loops” provide a differential gain of about 500 with no hysteresis.

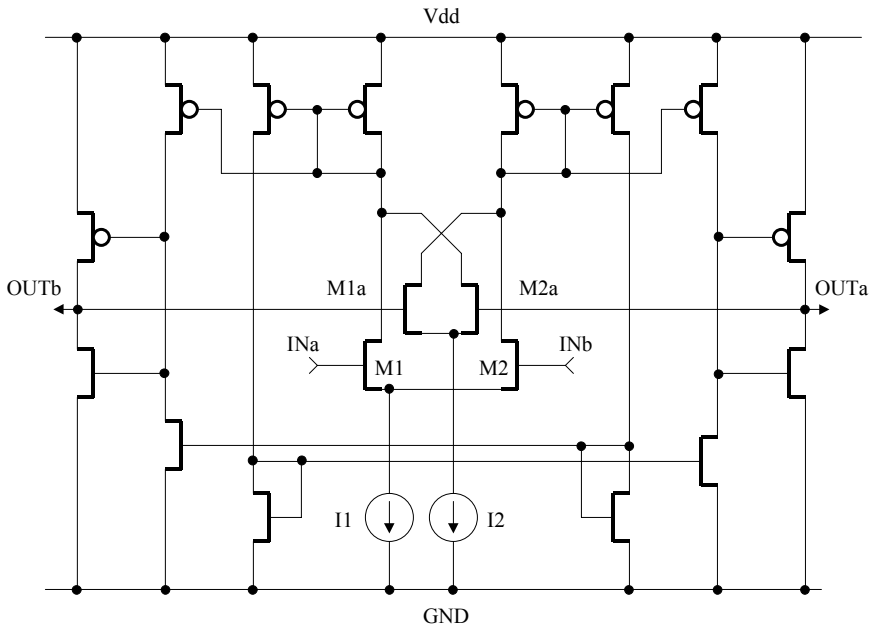


Figure 5. Discriminator simplified schematic

Hysteresis is provided by the M1a/M2a pair, which unbalances the static current through the main differential pair by a variable external current, shifting the effective discriminator threshold by up to 100 mV. The main bias current is provided by R1 (poly-resistor). The expected operating regime is at a threshold of about 20 primary electrons, which corresponds to a differential signal of about 300 mV at the discriminator input.

2.4.6 LVDS output cell

This cell, shown in Figure 6, provides an "LVDS-like" low-level logic output, with a nominal swing of 160 mV into 100 Ω centered at 1.2 V. This corresponds to the "reduced range link" described in IEEE 1596.3. [13].

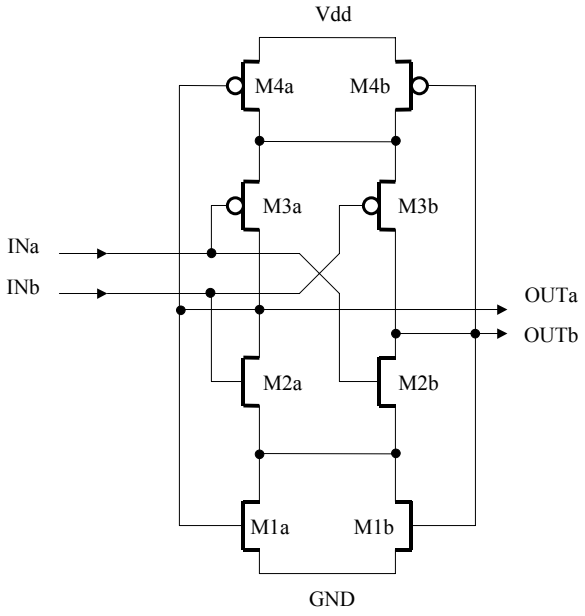


Figure 6. LVDS driver simplified schematic

Differential drive is provided directly from the discriminator outputs to two moderately-sized inverters (not shown). These inverters drive the output stage, which is essentially a pair of inverters (M2a/M3a and M2b/M3b) with their output current limited by transistor pairs (M1a/M1b and M4a/M4b) operating in their resistive region. Common-mode feedback from the outputs to the resistive FETs sets the common-mode output voltage.

The DC characteristics are set entirely by transistor sizes and are thus subject to process variations. Observations on fabricated devices from multiple prototype runs agree with Monte Carlo simulations and comply with the specification. Test results are provided in section 5.2.

2.4.7 Analog pad driver

Analog output is provided for channel 8 only for diagnostic purposes. The pad driver cell is shown in and is simply a set of cascaded source followers reminiscent of the old "Damn Fast" buffer parts from National Semiconductor.

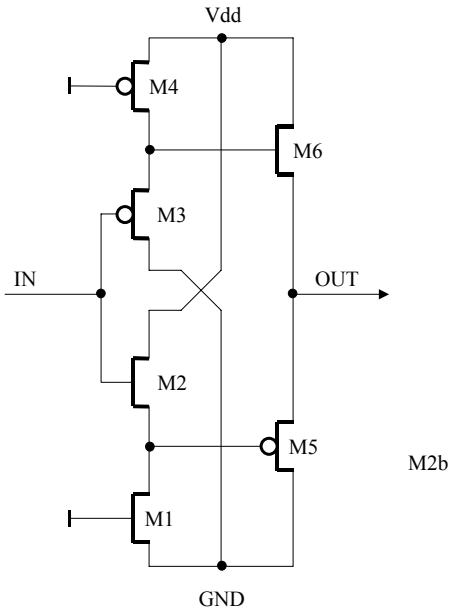


Figure 7. Analog pad driver simplified schematic

The gain of this cell is only about 0.5 when driving a high impedance load. It is capable of driving a terminated twisted pair but at lower gain. When back terminated with 50 Ω and driving a 50 Ω load, the circuit suffers a total of approximately 8:1 attenuation. Still, it is useful as an observation of MDT signal shape and provides an accurate means for noise measurements. It has a separate V_{DD} connection on the chip so that it can be powered down except for diagnostic purposes as desired.

2.4.8 Wilkinson ADC

The Wilkinson ADC serves as a time slew correction and also provides diagnostics for monitoring chamber gas gain. It operates by creating a gate of approximately 15 ns width at the leading edge of the signal, integrating the signal charge onto a holding capacitor during the gate, and then running down the hold capacitor at constant current. The rundown current is chosen so that maximum rundown time is of order < 200 ns. The scheme is shown in a simplified diagram in Figure 8.

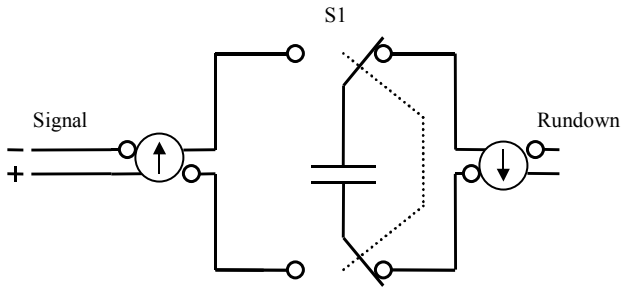


Figure 8. Wilkinson charge-to-time converter principle

The Wilkinson cell is fully differential and uses the same differential transconductor as the shaper stage as floating current sources, both for the integration current source as well as the rundown current sink. A discriminator, similar to the one used for the main threshold, is used to sense when the holding capacitor has run down to zero.

The gate generator logic is shown below in the block diagram in Figure 9.

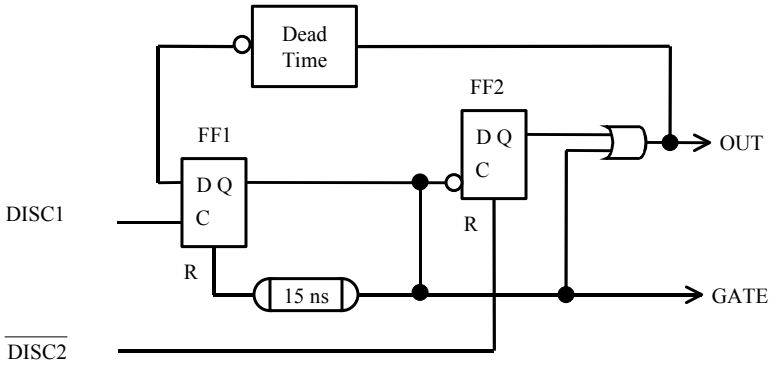


Figure 9. Gate generator block diagram

The main discriminator, DISC1, fires a one-shot consisting of flip flop FF1 and a 15 ns delay element thus generating the Wilkinson GATE signal. Delay elements are based on complementary current sources charging appropriately sized capacitors driving logic gates with hysteresis. The trailing edge of the GATE signal fires a second flip-flop, FF2, resulting in the OUT signal. This, in turn, activates the run down current which eventually discharges the hold capacitor and is sensed by discriminator DISC2. This in turn, resets FF2, and terminates the cycle. Further input signals are inhibited by the "dead time" delay element which is programmable up to approximately one microsecond.

2.4.9 Input protection

Primary input protection is provided by a pair of large N+ diodes in series with a wide 3 Ω input resistor. The resistor is a silicide blocked polysilicon resistor attached directly to the input pad. Each diode consists of eight fingers of n+ diffusion, 50 microns each, surrounded by P+ diffusion for a total finger length of 400 microns. The whole structure is surrounded by an additional N+ diffusion which acts as the collector of an npn structure. The collector scoops up current discharged into the substrate more effectively than the P+ cathode strips alone. Each such diode has a total capacitance, area plus fringe, of about 0.8 pF.

There is also a smaller pair of P+ diodes connected to the positive supply rail. In principle, a human body model type discharge into these diodes would dump current into the positive supply rail which, therefore, requires a clamp for bare chip handling. This clamp is based on the UMC "Corner" design [14], but is a bit simpler. It is by no means, guaranteed to withstand a full HBM discharge while the device is unconnected.

While these diodes are robust, they are not sufficient to withstand a full 3 kV – 4 kV MTD chamber discharge which can be of order several amperes. Additional off-chip protection in the form of back to back 1N914 signal diodes, in conjunction with the on-chip diodes, has been shown to provide robust protection against such discharges.

All digital I/O pads are taken from the MOSIS Hi-ESD Pad Library for the HP AMOS14B process [15].

2.5 Subcircuit characteristics

2.5.1 Pre-amplifier

Figure 10 shows the simulated signal transfer characteristic of the ASD pre-amp. The input signal is a voltage step function with a rise time of 2 ns applied to an ideal capacitor of 100 fF at the pre-amp input. The range is 50 – 800 mV yielding a charge range of 10 – 160 fC. The small signal frequency response of the pre-amplifier is shown in Figure 11. The input signal is a 1 mV AC signal.

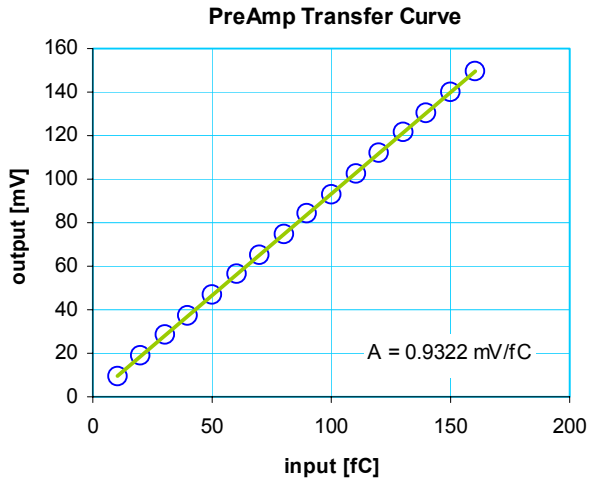


Figure 10. MDT-ASD pre-amplifier: SPICE simulation of the transfer characteristic (output peak voltage vs. input charge) shows good linearity over an extended input charge range (Nominal range ~ 10 – 80 fC). The gain is 0.93 mV/fC.

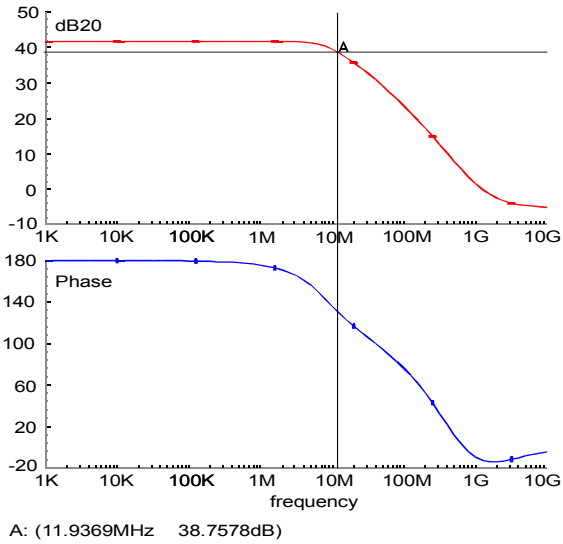


Figure 11. MDT-ASD pre-amplifier frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of 41.75dB with the -3dB point at 11.94 MHz. The rolloff slope is -6dB/octave. The phase plot shows an initial phase shift of 180°, decreasing to zero at ~ 700 MHz.

2.5.2 Differential amplifier stages DA1 through DA4

Four differential amplifier stages DA1 through DA4 serve both as gain and as shaping amplifiers. The basic topology for all four amplifiers is identical while the feedback networks differ according to the desired frequency characteristics.

- DA1 is a simple gain stage with purely resistive feedback. The bandwidth is limited by the product of the feedback resistor and the load capacitance, typically consisting of the gate capacitances of the subsequent stages and the source/drain capacitances of the input and output transistor pairs. The gain is 4.5dB with a 3dB bandwidth of 45 MHz (Figure 13). The pulse peak voltage gain is in the order of 1.1 exhibiting sufficient linear behavior (Figure 12). DA1s main purpose is to ensure the signal being completely complementary.

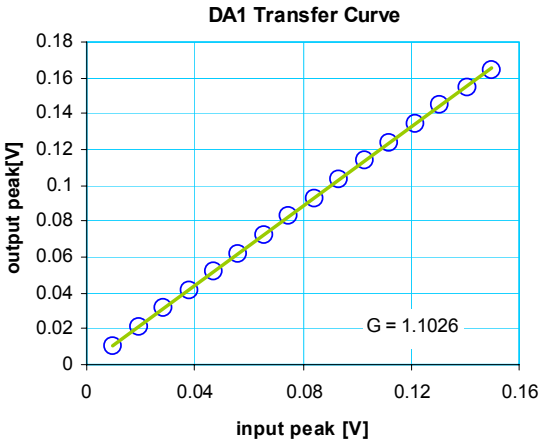


Figure 12. Differential amplifier DA1: Output versus input pulse peak voltage. The linear region extends the working signal range by at least a factor of two.

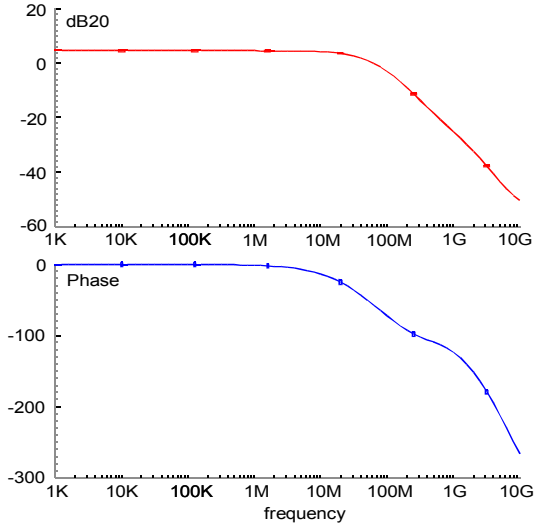


Figure 13. Differential amplifier DA1 frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of 4.5dB with the -3dB point at 45 MHz. The rolloff slope is -6dB/octave. The phase plot shows an initial phase shift of 0°, decreasing to -180° at ~ 3 GHz.

- DA2 and DA3 constitute the shaping portion of the MDT-ASD. The desired combined shaping function has a bipolar characteristic. This frequency response is achieved by adding a series R-C branch in parallel to the resistive feedback in case of DA2 and by replacing the feedback resistor with a series R-C branch in DA3.
  DA2 shows a linear voltage gain of 3.4 over the extended signal range (Figure 6) while DA3 exhibits a compressive transfer characteristic with a small signal voltage gain of ~ 3.2 [3]. Again, the working signal range is roughly the first half of the plotted range.

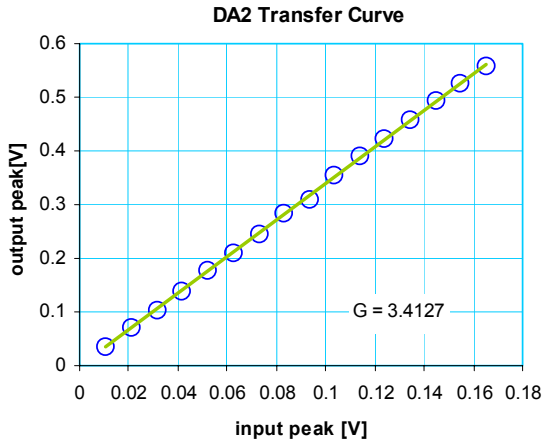


Figure 14. DA2 output peak voltage vs. input peak voltage The voltage gain of 3.4 (10.6dB, compare Figure 16) is linear over the extended dynamic range.

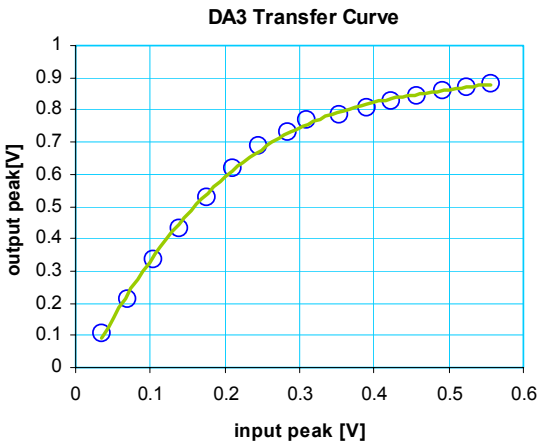


Figure 15. DA3 output peak voltage vs. input peak voltage. The small signal voltage gain is ~ 3.2 (~ 10dB, compare Figure 17). The transfer curve shows a compressive characteristic.

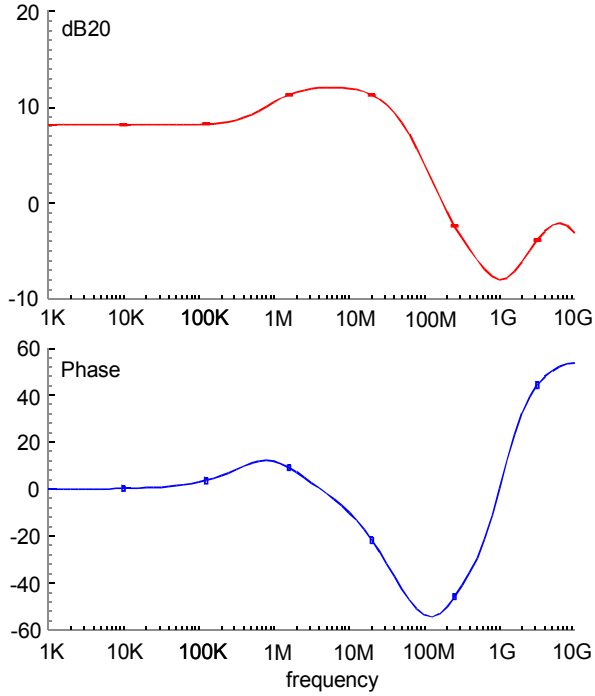


Figure 16. DA2 AC characteristics. The voltage gain peaks at ~ 11dB @ 5 – 10 MHz, the roll-off slope is –18dB/octave.

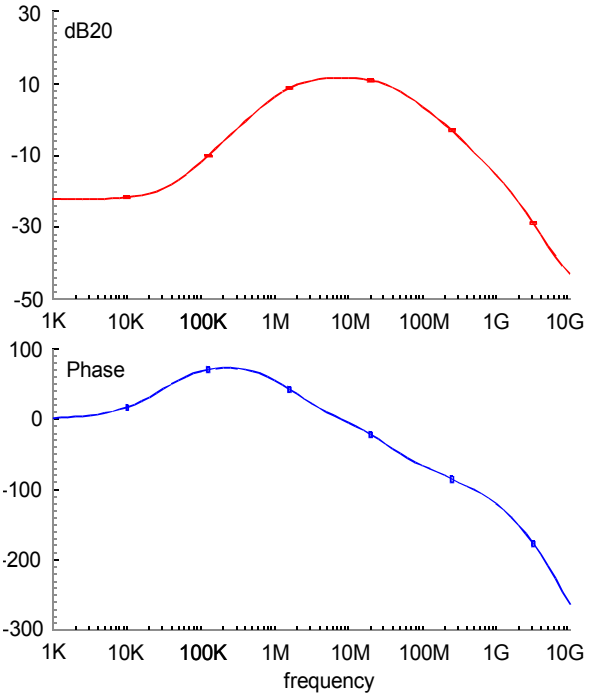


Figure 17. DA3 AC characteristics. The voltage gain peaks at ~ 10dB @ 5 – 10 MHz, the roll-off slope is -12dB/octave.

The AC characteristics of the shaping amplifiers are shown in Figure 16 and Figure 17. The gain peak for both amplifiers is approximately 10dB in the range of 5 to 10 MHz.

- DA4 is the pre-discriminator gain stage of the timing discriminator with a voltage gain of 5 to 6 (16dB). The transfer curve, again covering twice the expected signal range, shows DA4 going to saturation very fast.

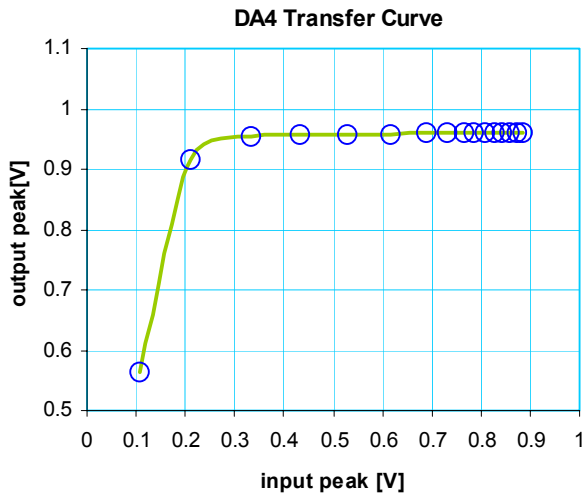
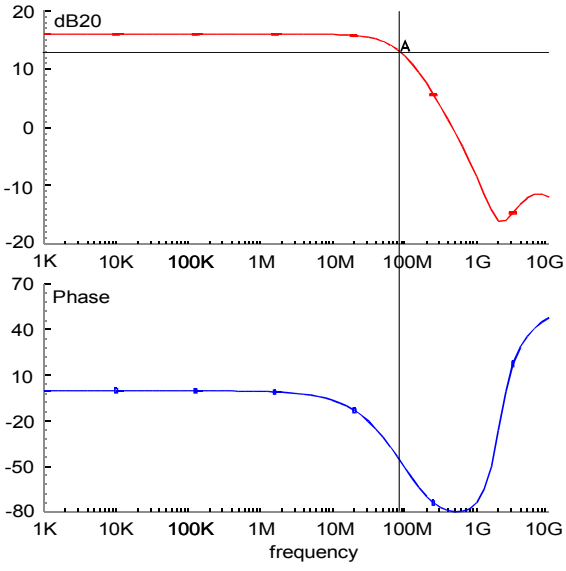


Figure 18. Differential amplifier DA4: Output versus input pulse peak voltage (double dynamic range).



A: (85.6677MHz 12.9881dB)

Figure 19. Differential amplifier DA4 frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of 16dB with the -3dB point at 86MHz. The rolloff slope is -6dB/octave. The phase plot shows an initial phase shift of 0° decreasing to -80° at 400 MHz.

2.5.3 Pre-Amplifier – Shaper: Combined transfer characteristic

The analog signal chain ends at DA3 output where the signal is tapped to be sent to the analog pad drivers and where the discriminator threshold is applied before the signal is put onto the pre-discriminator amplifier DA4. The combined characteristics of the pre-amplifier – shaper chain are summarized in Figure 20 and Figure 21.

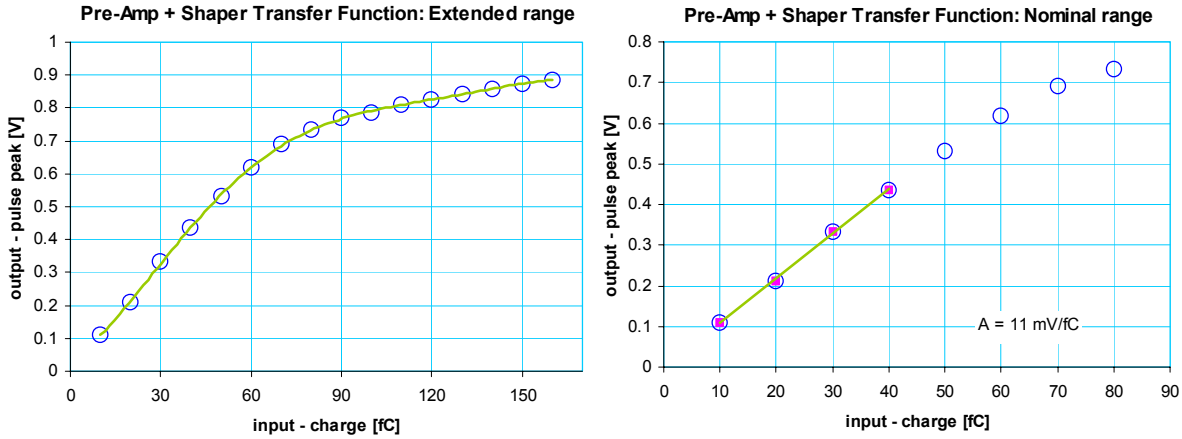


Figure 20. Analog signal chain transfer characteristics: Extended (left) and nominal range (right). The linearity within the nominal range is adequate. The sensitivity of the pre-amp – shaper combination is 11 mV/fC.

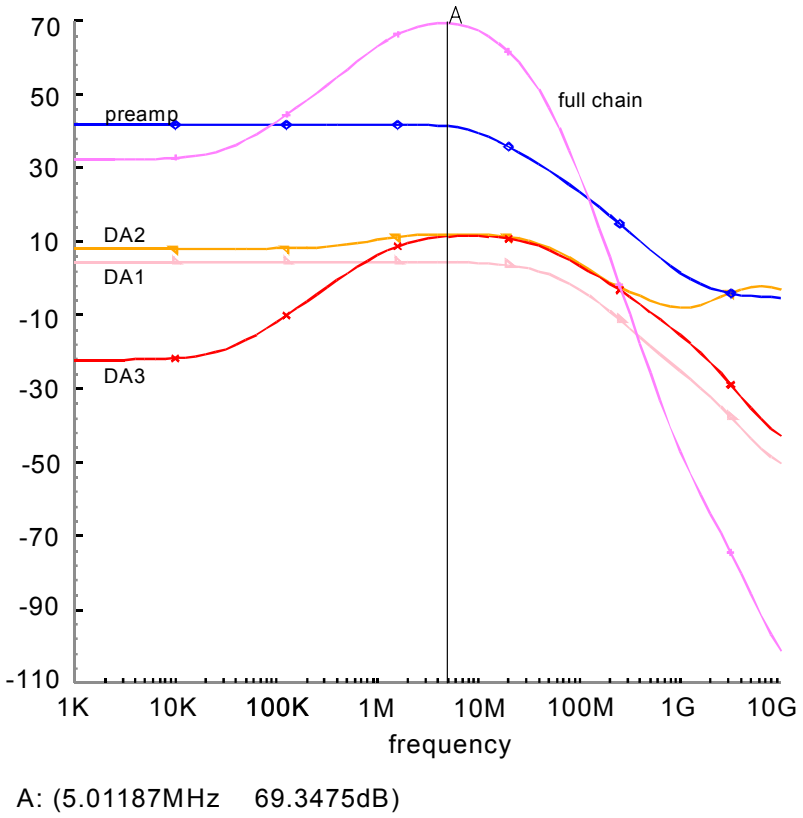


Figure 21. Pre-amplifier – DA3 analog signal chain: AC frequency response; the amplifier chain exhibits a pass-band characteristic with a center frequency of 5 MHz. The high-pass part, mainly imposed by DA3, shows a corner frequency of 30 kHz and a slope of +6dB/octave (representing a first order high-pass filter). The low-pass section is a superposition of all four amplifier low-pass characteristics that have similar corner frequencies between 38 MHz and 44 MHz. The curve shows a -24dB/octave slope (or 4th-order low-pass filter behavior) above ~ 45 MHz. At approx. 500 MHz where DA2 goes flat again, the slope reduces to -18dB/octave (3rd order). The peak lies at 5 MHz showing a gain of close to 70dB.

2.5.4 Pre-Amplifier – Shaper: Time domain pulse response

Figure 22 shows the response of the amplifier chain to current Delta pulses (a) at the pre-amp input, (b) shows the pre-amplifier signal, (c) and (d) are the outputs of the differential amplifiers DA1 and DA2 respectively. The threshold is applied at the output of DA3 (e), the DA4 signal (f) is fed into the discriminator.

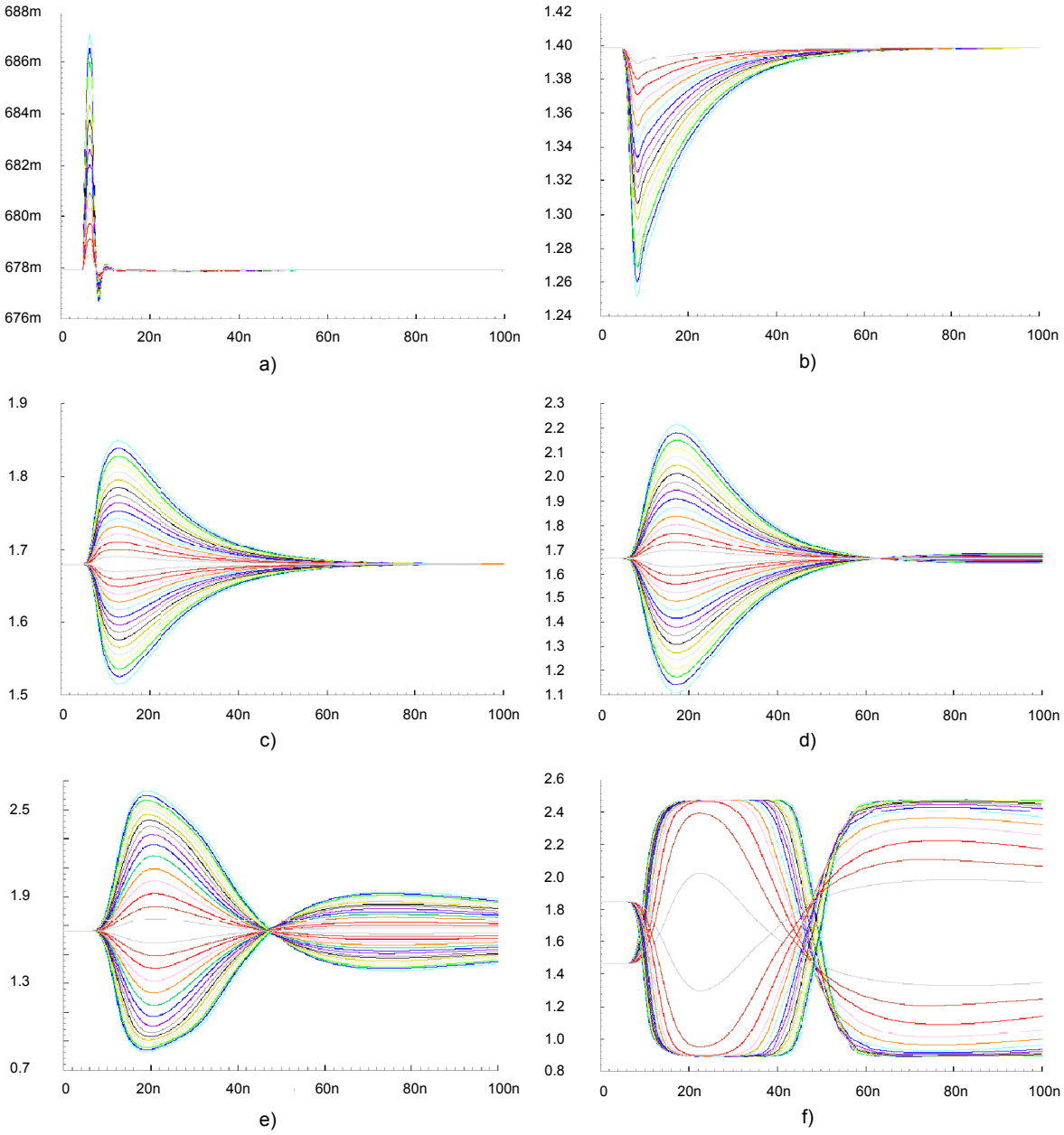
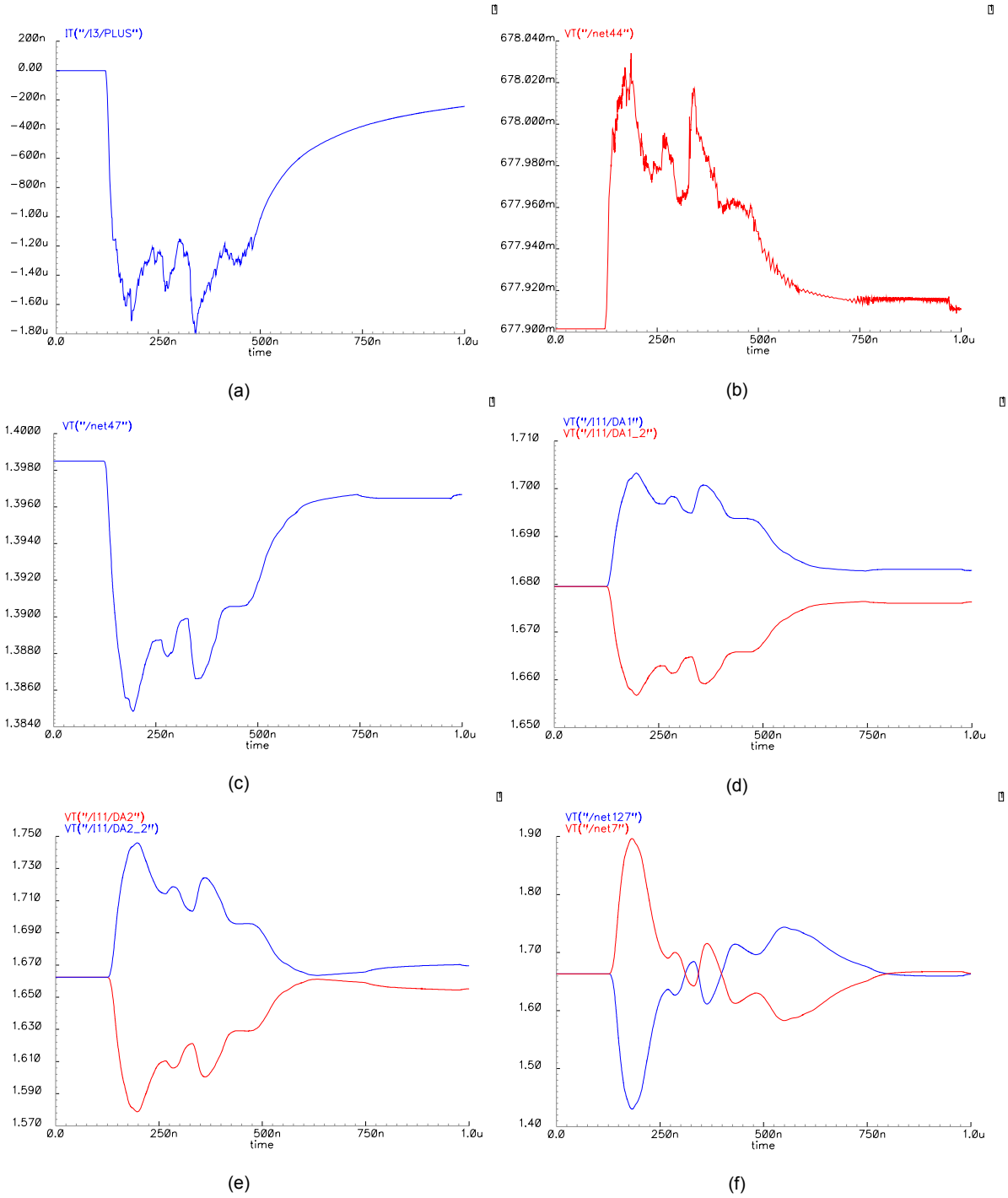


Figure 22. Spice simulation of the Delta pulse (a) response of the analog signal chain after the pre-amp (b), DA1 (c), DA2 (d), DA3 (threshold coupling point) (e) and DA4 (pre-discriminator gain stage) (f).

2.5.5 Simulation with GARFIELD signals

GARFIELD is a program for the detailed simulation of two-dimensional drift chambers, although drifting of particles, including diffusion, avalanches and current induction is treated in three dimensions [10]. The software package allows to create typical MDT signals which can be used within a Spice simulator.

Figure 23 shows the current induced on a MDT wire as seen at the tube's signal pin; (b) is the voltage at the ASD input pad assuming a simple electrical model of the tube including the termination resistor as well as coupling and parasitic capacitances; (c) shows the pre-amplifier output, (d), (e) and (f) the 3 differential amplifier outputs DA1 – DA3; (g) is the DA3 signal with a 60 mV nominal threshold applied; (h) shows the DA4 signal and the discriminator output.



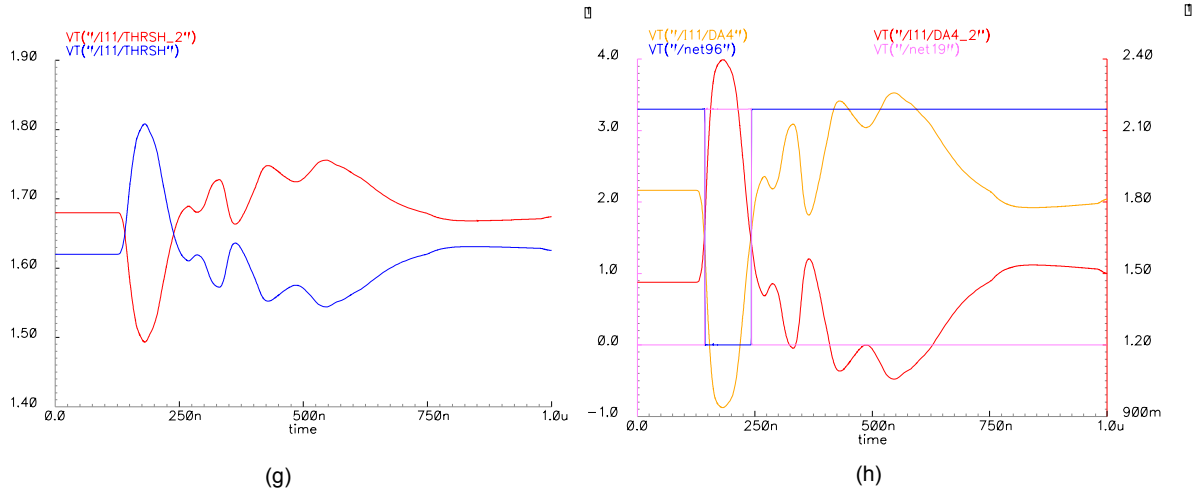


Figure 23. Response of one ASD channel to a MDT current signal created by GARFIELD [10].

2.5.6 Wilkinson ADC

The main purpose of the Wilkinson ADC is to provide data which can be used for the correction of time-slew effects due to pulse amplitude variations by measuring the charge contained in the rising edge of the MDT signal [7][9]. Time slewing correction improves the spatial resolution of the detector. In addition, this kind of charge measurement provides a tool useful for chamber performance diagnostics and monitoring. Further applications such as *dE/dx* measurements of slow moving heavy particles like heavy muon SUSY partners etc are conceivable.
The result of the charge measurement is converted into time, encoded in the width of the output pulse. The information contained in the pulse, namely the leading edge timing and the pulse width encoded charge, will be read and converted to digital data by a TDC [1].

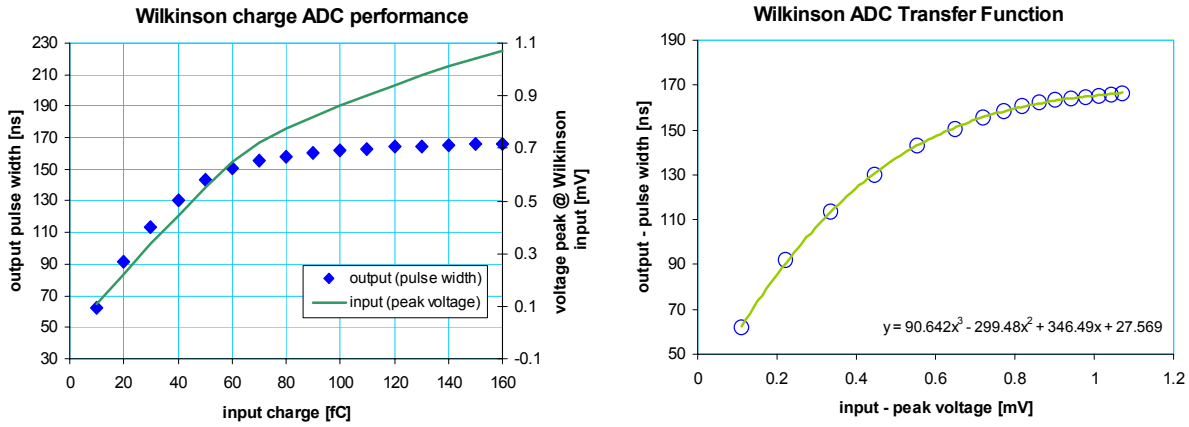


Figure 24. Spice simulation of Wilkinson ADC characteristics. The left-hand plot shows the width of the output pulse (simulated) and peak voltage at the ADC input as a function of the input signal charge. Consequently this plot includes both the non-linearities of the amplifier chain and the converter. It has to be noted that the plots cover a largely extended input signal range. The expected working range will be in the area of ~ 20 – 80 fC. The right-hand plot shows the converter transfer characteristic (ADC output vs. input). All simulations were done with the following parameter settings: Integration gate 17 ns, DISC2 threshold 64 mV, discharge current 1.6 µA. (see section 2.6.1.3 for adjustable parameters of the Wilkinson ADC).

Figure 25 shows the response of the Wilkinson ADC to the GARFIELD signal of the last section. The two digital signals are the integration gate (16 ns) and the rundown gate (~ 55 ns). The ADC output pulse is constructed as the OR disjunction of the two gates. The rundown current was set to a medium value. The differential analog signal shows the triangular shape composed of the integration and the run-down ramp. The end of the conversion cycle is triggered by the rundown ramps undershooting the threshold of a second discriminator (DISC2).

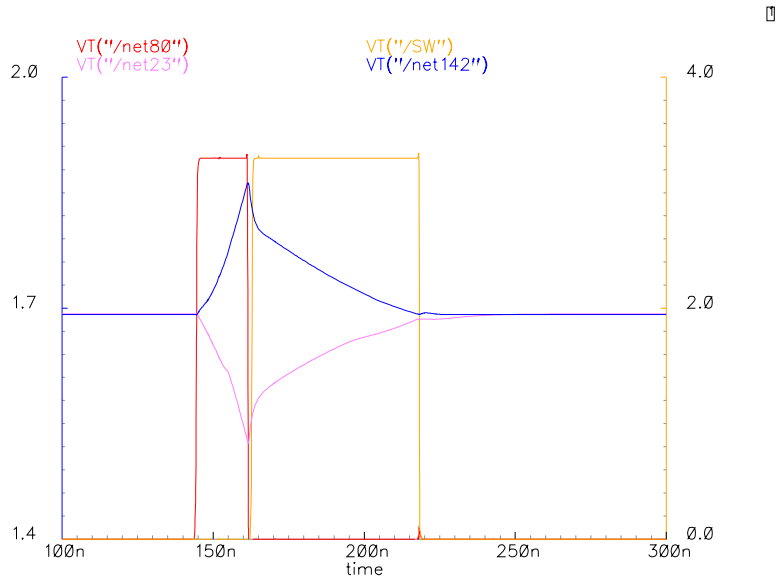


Figure 25. Wilkinson ADC: Internal ramp signals and gate signals (integration gate and rundown gate). The ADC output pulse is constituted by the OR disjunction of the two gate signals.

2.5.7 Analog pad driver

The pad driver has a voltage gain of –3.7dB and a bandwidth of 185 MHz (Figure 26).
Figure 27 shows the voltage of the analog output pulse peak measured at the analog output pad as a function of the input charge. The discrepancy between simulation and measurement is small which indicates that the used simulators and device models are reasonably accurate. The differences can also be caused by numerous other effects, including variations of process parameters. Measurement results assuming the on-chip calibration capacitors being 10% below designed value are added for illustration (solid blue line).

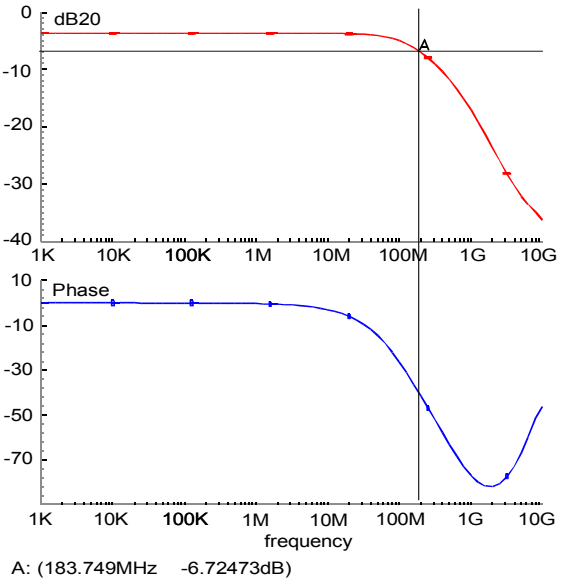


Figure 26. Analog pad driver frequency response – gain and phase Bode plots: The amplifier shows a small signal gain of -3.7dB with the -3dB point at 184 MHz. The rolloff slope is -6dB/octave.

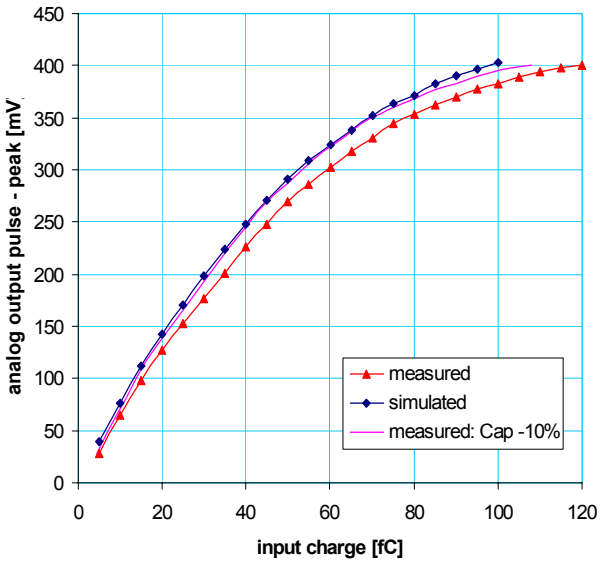


Figure 27. Simulated and measured analog output pulse peak versus input charge using the calibration injection system. The blue solid line represents measurement results assuming the on-chip calibration capacitors being 10% lower than their designed value.

All simulations were done using BSIM3 Version 3.1 Level 49 MOS transistor-models[2] and the AVANT® HSPICE simulator (Star-HSPICE 98.2.1 [980912])

[2] The transistor models used in all simulations are listed in the appendix

2.6 Programmable parameters

It was found advantageous to be able to control or tune certain analog and functional parameters of the MDT-ASD, both at power-up/reset and during run time. Rather than applying external currents or voltages, it was chosen to send the control signals as digital data to the chip, where they are converted into physical quantities by custom Digital-to-Analog Converters (DACs) as required. A serial I/O data interface was implemented in the ASD, containing digital I/O ports, shift registers plus shadow registers and the required control logic (see 2.6.2 below). The data as well as the control signals and the shift register clock are generated by an FPGA[3] controller on the mezzanine card and are transmitted to the ASDs using a JTAG like protocol.

Table 4 gives a summary of all programmable parameters including their nominal/default settings, range, resolution/LSB and number of bits. The total number of control bits/ASD chip is 53. A power-up/reset routine, which loads the ASD registers with the nominal values of Table 4 will be incorporated in the JTAG controller[4].

Table 4. Summary of programmable parameters

Parameter	Nominal value	Range	LSB	Units	Resolution	bit
DISC1 Threshold	60	-256 – 256	2	mV	256	8
DISC1 Hysteresis	10	0 – 20	1.33	mV	16	4
Wilkinson integration gate	16	11 – 21	0.625	ns	16	4
DISC2 Threshold	32	32 – 256	32	mV	8	3
Wilkinson discharge current	1.3	1.1 – 2.4	0.1857	μA	8	3
Dead-time	800	300 – 1000	100	ns	8	3
Calibration channel mask	–	–	–	–	–	8
Calibration capacitor select	–	50 – 400	50	fF	8	3
Channel mode	ACTIVE	–	–	–	–	16
Chip mode	ADC	–	–	–	–	1

Total number of bits: 53

2.6.1 Programmable analog parameters

2.6.1.1 Timing discriminator threshold

The threshold for the timing discriminator (DISC1) is applied at the AC coupled input of the pre-discriminator differential amplifier (DA-4). As the signal path is fully differential, we use two complementary 8-bit dual resistor divider voltage-DACs with an output swing of $V_{base} \pm 128$ mV where V_{base} is nominally VDD/2. One of the DACs receives an inverted set of control signals. Consequently the potential difference between both DAC outputs, corresponding to the applied threshold, can vary from 256 mV through zero to –256 mV. The nominal threshold setting is $V_{base} \pm 30$ mV (60 mV effective threshold). Refer to [7][8][9] for the determination of optimum threshold levels. Positive and negative reference potentials are supplied by bootstrap type voltage references.

Table 5 summarizes the main design parameters of the voltage DAC.

Table 5. Main threshold DAC properties

Parameter	Definition	Value	Units
Type	VDAC	–	–
Range	$V_{RP} - V_{RN}$	256	mV
Resolution	N bits	8	–
LSB	$(V_{RP} - V_{RN})/2^N$	1	mV
Differential non-linearity	$MAX(V_{n+1} - V_n) - LSB$	< 1	mV
Integral non-linearity	$MAX(V_n - V_{n,ideal})$	< 5	mV
Monotonicity	$V_n \le V_{n+1}\ \forall\ n$	√	–
No Missing code	$V_n \ne V_{n+i}\ \forall\ n, i$	√	–

[3] The FPGA may be replaced by an ASIC or the functionality transferred to the TDC (AMT-2).
[4] It exists also the option to implement this feature on the ASD chip itself.

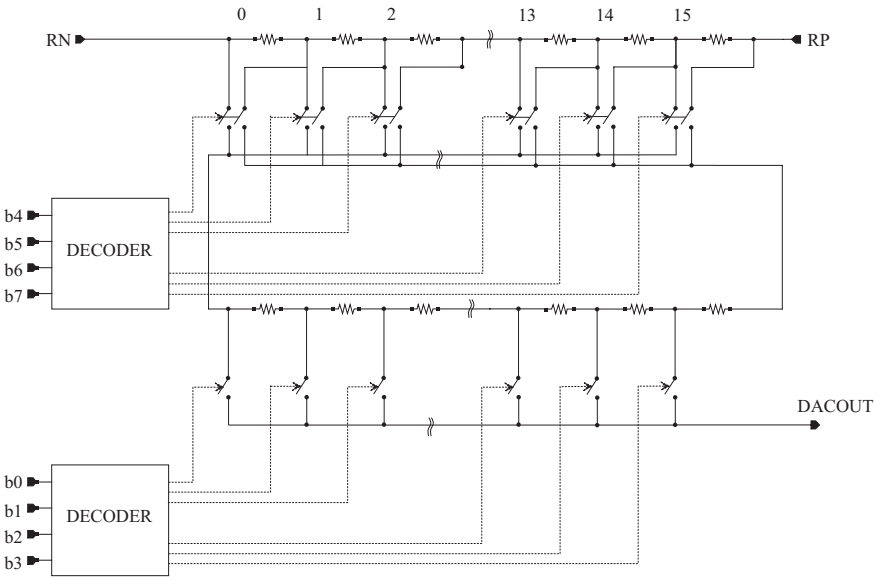


Figure 28. Block schematic of the 8-bit main discriminator threshold voltage DAC

2.6.1.2 Timing discriminator hysteresis

It was demonstrated that the option of a wide-range adjustable hysteresis for the timing discriminator is a useful feature to reduce the probability of multiple threshold crossings in the tail of the MDT signal [7][8][9]. It also improves the system reliability by removing ambivalent output states of the discriminator due to signals or signal fluctuations close to the threshold level.

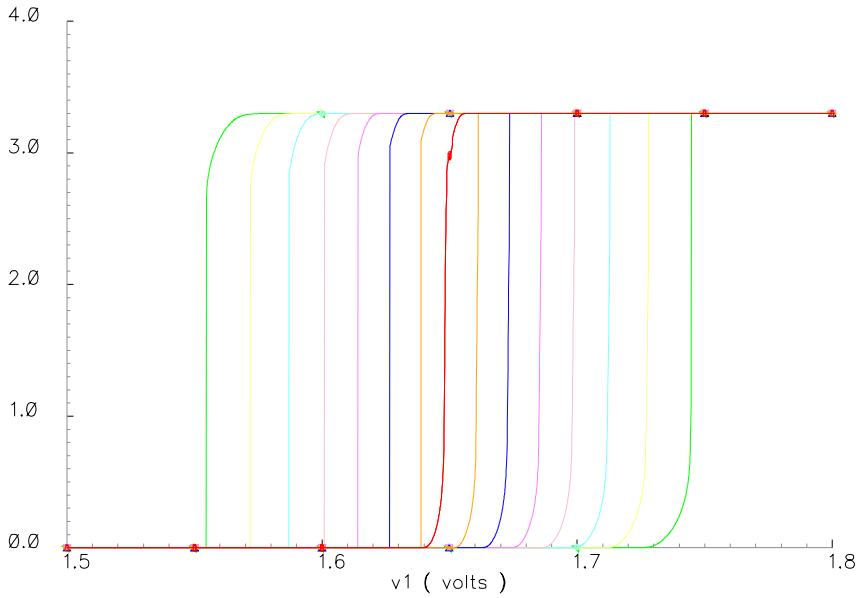


Figure 29. Simulation of the timing discriminator output vs. input voltage DC sweep for the eight different Hysteresis-DAC settings

The hysteresis for DISC1 is applied through a scaled-transistor current source DAC with a resolution of 4 bits. The range of the DAC is 320 µA with a LSB of 40 µA. This corresponds to a hysteresis voltage range of 0 – 20 mV at the threshold coupling point DA–4 (0 – 7 primary electrons) or 0 – 100 mV at the discriminator.

2.6.1.3 Wilkinson ADC Control

- The **integration gate width** can be set from 11.5 ns to 34 ns in steps of 1.5 ns (4-bit). This setting influences what fraction of the leading edge charge of the signal is used for time slew correction. The nominal gate width is 16 ns which corresponds to the average peaking time t_p of the pre-amplifier. It can be demonstrated that the time slewing is only correlated to the leading edge charge and not to the total signal charge of the MDT signal. ADC measurements with a gate $> 2 \times t_p$ thus can not be used to further improve the spatial resolution of the system [7], [8], [9]. The current controlling the gate width is set by a binary-weigthed switched resistor string.

- The **threshold** is applied to the differential threshold terminals of the Wilkinson discriminator (DISC2) by two coupled resistor divider voltage DACs with 3-bit resolution and a range of 16 mV to 128 mV (LSB = 16 mV). One set of control signals sets both DACs complementary. Unlike DISC1 threshold, the two DACs do not cover the same range. The range of the positive going DAC is V_{base} + 16 mV to V_{base} + 128 mV, the one of the negative from V_{base} − 16 mV to V_{base} − 128 mV. The minimum threshold thus amounts to 32 mV. The same voltage references as for the DISC1 threshold DACs are used. The DISC2 threshold also affects the width of the Wilkinson ADC output pulse (see below) but does not influence the ADC performance in a wide range and is primarily implemented for troubleshooting and fine-tuning purposes.

- The **discharge (rundown) current** of the integration capacitors is set by a binary-weigthed switched resistor chain in a range between 1.1 µA and 2.4 µA (3-bit). This allows the ADC output pulse width to be adjusted to the dynamic range of the TDC (200 ns @ resolution 0.78125 ns). This pulse width range (caused by the MDT signal amplitude range) is jointly determined by the integration gate width, the DISC2 threshold and the discharge current. For nominal settings (integration gate: 16 ns, DISC2 threshold: 32 mV complimentary) and a typical input signal, the ADC output can be set between 85 ns and 135 ns by controlling the rundown current. The nominal setting (1.3 µA) yields a 110 ns output pulse. The dynamic range (input signal from "just-above-threshold" to saturation) of the ADC output appears at these nominal settings to be 40 ns – 140 ns (100 ns range ⇒ 7-bit TDC resolution). See 2.5.5 for simulated Wilkinson ADC performance.

- The **deadtime** setting defines an additional time window after each hit during which the logic does not accept and process new input. It can be set from 300 to 1000 ns in steps of 100 ns (3 bit). The nominal setting is 800 ns corresponding to the maximum drift time in the MDT. This feature can be used to suppress spurious hits due to multiple threshold crossings in the MDT signal tail (additionally facilitated by the bipolar shaping scheme). The deadtime window is added to the output pulse, thus a minimum deadtime is always present (the time of the output pulse itself). The current controlling the dead time is set by a binary-weigthed switched resistor string.

Different combinations of the ADC settings affect the output pulse in a wide range. For minimum integration gate (11 ns), high rundown current (2.5 µA) and high DISC2 threshold (128 mV), the width of the pulse can go as low as 15 ns for a very small input signal. The other extreme (gate 34 ns, rundown current 1µA, DISC2 threshold 16 mV) yields a 240 ns ADC output pulse for a large signal (note that certain settings exceed the TDC dynamic range). Figure 30 shows the ADC output pulse width for three different integration gate settings as functions of the rundown current. The output pulse widths lie within the shaded areas depending on input signal charge and rundown current setting.

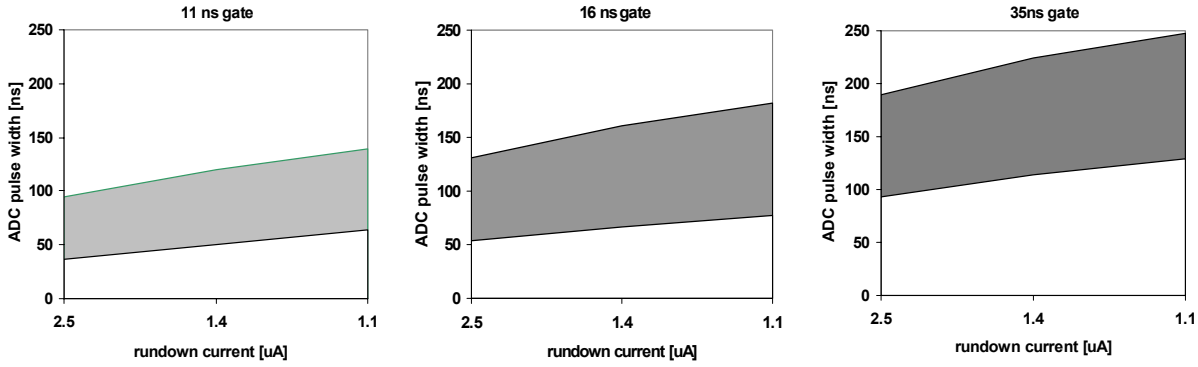


Figure 30. Influence of integration gate and rundown current settings on the ADC output pulse width.

2.6.2 Programmable functional parameters

2.6.2.1 Calibration/test pulse injection

In order to facilitate chip testing during the design phase as well as to perform system calibration and test runs with the final assembly, a calibration/test pulse injection system was integrated in the chip. It consists of a parallel bank of 8 switchable 50 fF capacitors per channel and an associated channel mask register (Figure 31). The mask register allows for each channel to be selected separately whether or not it will receive test pulses. The capacitors are charged with external voltage pulses, nominal 200 mV swing standard LVDS pulses, yielding an input signal charge range of 10 – 80 fC.

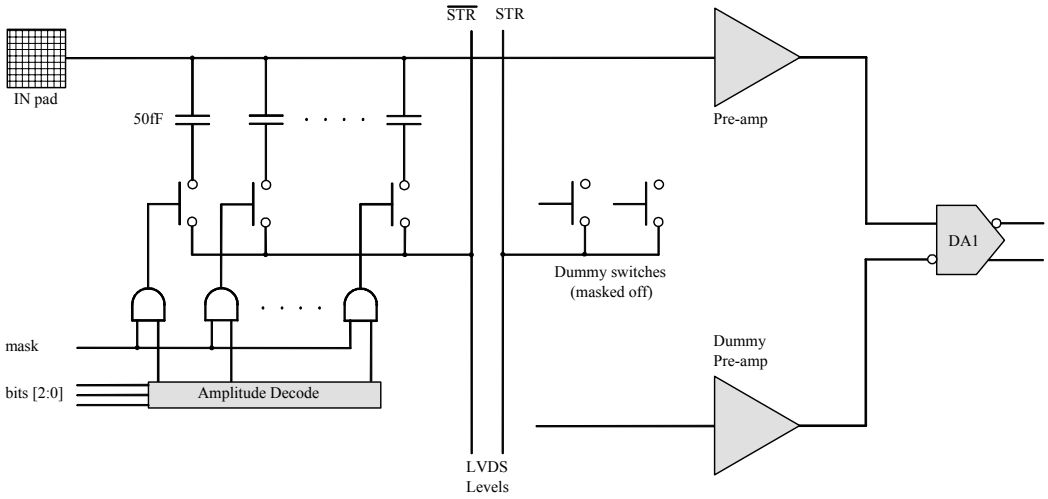


Figure 31. Calibration/test pulse injection – block diagram

2.6.2.2 Chip mode

One bit is used to set the global output mode of the MDT-ASD. The two modes are:

ADC mode (default)	In this mode, the output pulse width represents the charge measured in the leading edge of the MDT signal (pulse width encoded charge measurement, see section "Wilkinson ADC control"). The rising edge contains the timing information.
TOT mode (Time-over-Threshold)	In this mode, the discriminator signal itself is sent to the output drivers. Thus the width of the pulse is determined by the shape and amplitude of the MDT signal. Multiple threshold crossings (and output pulses) are possible. The rising edge of the first (main) pulse contains the timing information for the event.

2.6.2.3 Channel mode

For diagnostic (boundary scan) and troubleshooting purposes, the output of each channel can be set to one of three states (2 bits per channel):

ACTIVE	Channel on. Default working setting.
HIGH	LVDS output of the respective channel is forced HIGH ('Logic 1') (regardless of what happens in the analog part of this channel).
LOW	Like above but 'Logic 0'. These two settings allow boundary scan type connectivity checking of the circuit board. Particularly useful for large scale production testing.

2.7 Serial data interface

2.7.1 Architecture

The chosen ASD serial data interface architecture employs separate shift and working registers. The shift register is connected directly to digital input and output pads respectively. Its length is designed to hold a complete set of control bits (53). The data can be uploaded any time (asynchronously) to the shadow registers, which control the DACs, multiplexers etc. The architecture allows downloading the whole set of active bits from the shadow to the shift register in order to send them back to the controller for diagnostic or monitoring purposes. This can be done any time and does not interfere with the normal operation of the ASD. The interface, for each data bit, consists of the shift register-cell, implemented as a static master-slave D flip-flop, the shadow register cell, realized as a static transparent latch and 2 two-in-one multiplexers (Figure 32). ASDs thus can be daisy-chained to form a closed JTAG type control loop.

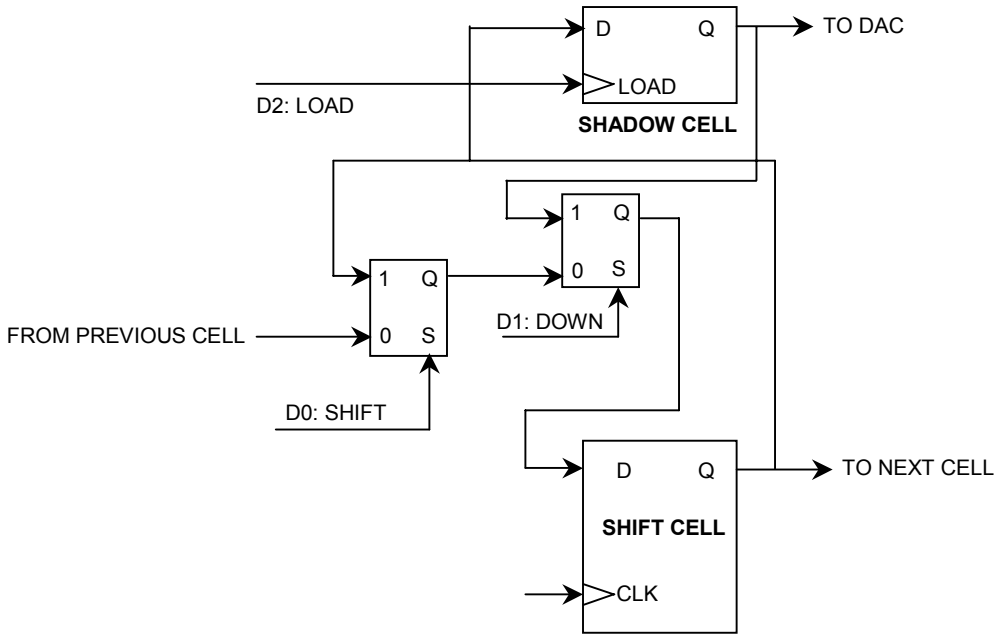


Figure 32. Serial data interface

2.7.2 I/O operation

The protocol requires 2 data lines (TO and FROM chip), 3 control lines (SHIFT [D0], DOWN [D1], LOAD [D2]) and one clock line (Table 6). The configuration allows extensive control over the data flow (Table 7). HOLD mode keeps the data in the shift register by feeding back each cell with its own content. SHIFT mode shifts data right at the rising edge of the clock. LOAD active copies the bits in the shift register to the shadow register at any time (asynchronous). DOWN active copies the contents of the shadow registers to the shift register at the next rising clock edge (overrides SHIFT – HOLD). The ASD serial input expects the data to be stable at the rising edge of the clock ± a few nanoseconds. The controller will change data bits at the falling clock-edge. Thus data are stable at the input for the entire clock period with the sensitive rising edge in the middle. Data bits at the ASD serial data output also change state at the falling edge of the clock.

Table 6. Serial interface signal lines

DATA_IN	Data line from controller to ASD shift register input
DATA_OUT	Data line from ASD shift register output to controller
CLK	Clock line
D[0:2]	Register control lines

Table 7. Serial interface instruction encoding

Instruction	D0	D1	D2	Operation
SHIFT	1	0	X	Shift right at rising edge of CLK
HOLD	0	0	X	Keep shift register contents (self feedback)
DOWN	X	1	X	Copy contents of shadow register to shift register @ rising edge of CLK
LOAD	X	X	1	Load shadow registers with contents of shift register (asynchronous)

Shift and shadow registers have a length of 54 bits, where 53 are actual data bits. The last shift register cell is clocked with an inverted clock, making the output change at the falling edge of the clock. A DOWN instruction causes the last cell to perform a HOLD operation.

2.7.3 Shift register bit assignment

The bit assignment of the shift register is given in Table 8. JTAG bit 0 is the last bit to enter the shift register. Data words are loaded LSB first. Channel 1 is the top most channel when looking at the chip with the analog inputs on the left-hand side. The mask bit for channel 1 is JTAG bit 0. The DACs for Rundown Current and DISC2 Threshold give the lowest output for all bits set. All other DACs vice versa.

Table 8. Shift register bit assignment

JTAG bit #	Description	LSB/code
[0:7]	Channel mask register 1 – 8 [0:7]	bit 0 channel 1 (top)
[8:10]	Calibration injection capacitor select [2:0]	bit 10 LSB
[11:18]	Main threshold DAC (DISC1) [7:0]	bit 18 LSB
[19:21]	Wilkinson ADC threshold DAC (DISC2) [2:0]	bit 21 LSB
[22:25]	Hysteresis DAC (DISC1) [3:0]	bit 25 LSB
[26:29]	Wilkinson ADC integration gate [3:0]	bit 29 LSB
[30:32]	Wilkinson ADC rundown current [2:0]	bit 32 LSB
[33:35]	Deadtime [2:0]	bit 35 LSB
[36:37]	Channel mode – channel 1 (top) [1:0]	‘00’ ACTIVE ‘01’ HIGH ‘10’ LOW ‘11’ OFF
[38:39]	Channel mode – channel 2 [1:0]	
[40:41]	Channel mode – channel 3 [1:0]	
[42:43]	Channel mode – channel 4 [1:0]	
[44:45]	Channel mode – channel 5 [1:0]	
[46:47]	Channel mode – channel 6 [1:0]	
[48:49]	Channel mode – channel 7 [1:0]	
[50:51]	Channel mode – channel 8 (bottom) [1:0]	
[52]	Chip mode	‘0’ ADC, ‘1’ TOT

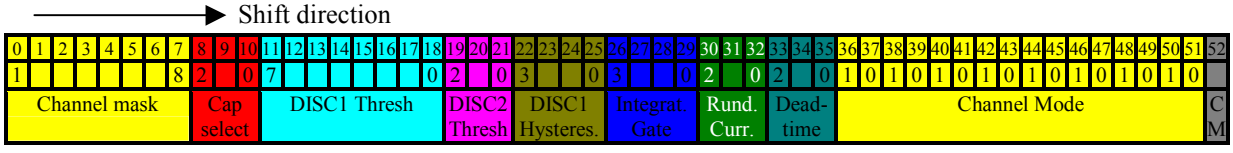


Figure 33. Shift register image

3 IC layout

3.1 Die and packaging

Eight channels of the ASD analog signal chain (Figure 1) and the serial I/O data interface plus DACs, registers and control logic for the programmable features are fabricated on a 3180 μm × 3720 μm die. The floor plan and the chip layout are shown in Figure 34. All analog inputs are placed on the left side of the chip while the LVDS outputs lie opposite. Top and bottom sides are taken by the digital I/O and the power supply pads. V_{DD} and Ground pins for the pre-amplifiers are replicated on the top side to prevent voltage drops along the power buses.

In order to enable/simplify testing and monitoring, the output voltages of all threshold DACs are connected to separate output pads. Additional testability is provided by an adequate number of probe pads at crucial points of the layout. These pads though are accessible only with a probe station.

The chip is packaged using a rectangular 80-pin PQFP80E package with the dimensions 14 mm × 20 mm and a pin pitch of 0.8 mm. A pin-out diagram and a bonding diagram plus additional information on the package can be found in appendix 5.3.

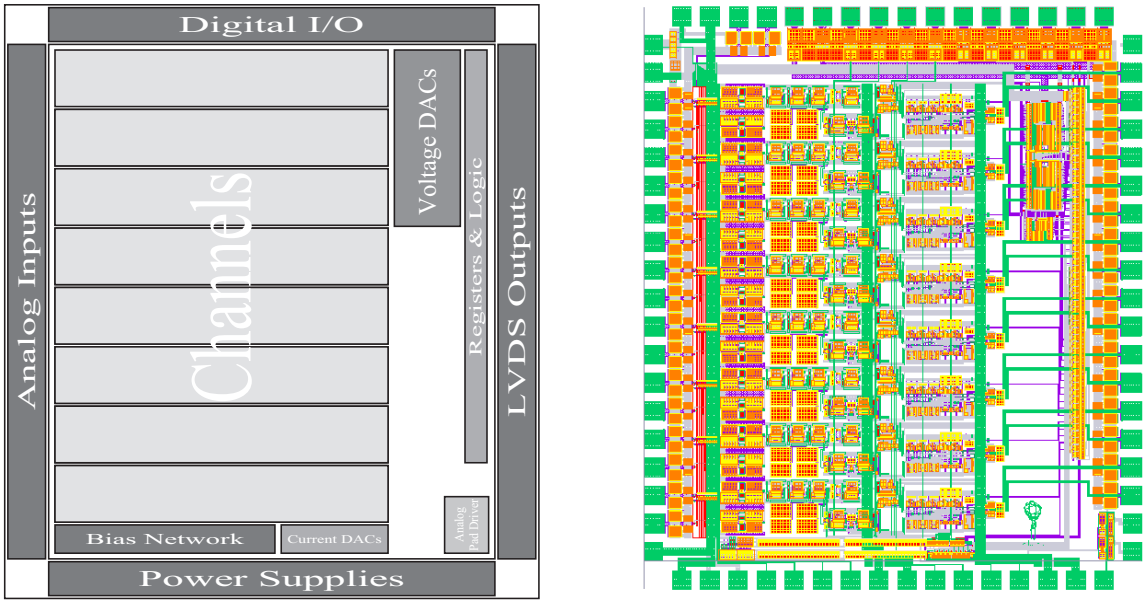


Figure 34. Octal MDT-ASD: Floor plan and chip layout for the HP 0.5 μm CMOS process

3.2 Substrate noise coupling

The MDT-ASD is a “mixed signal” ASIC and as such, careful attention must be paid to the issue of substrate noise coupling [11]. In particular, the Wilkinson Gate Generator subsection operates in essentially real time unlike the serial I/O programmable logic cells in the chip. This presents potential problems due to substrate coupled digital noise into the analog sections of the chip. To alleviate this potential source of coupling, the gate generator logic sub-cells are all custom built fully differential logic. Each rail-to-rail logic swing is accompanied by a complementary swing in close physical proximity. These pairs can induce considerable electric field lines into the substrate. To alleviate such effects, the logic cells are all heavily guard ringed to substrate nets which are tied off-chip to ground. These guard rings stabilize the substrate by terminating the noisy field lines from digital logic signals. Extensive testing has shown that coupling of these cells into the analog signal chain occurs at extremely low levels.

4 Prototyping

All sub-circuits and building blocks of the MDT-ASD were prototyped at different stages of the development. One of the prototypes, dubbed "ASD light", a reduced-functionality[5] 4-channel chip was produced in larger quantities to be used for MDT chamber production testing. The following sections contain test and measurement results taken from different prototype chips, though mainly from the final octal prototype ASD00A. All results are produced by the final sub-circuit versions as implemented on ASD00A and intended to be identical on the production version of the chip.

4.1 Performance and functionality testing

4.1.1 Analog output

Figure 35 shows the voltage of the analog output pulse peak versus input charge using the calibration injection system. The discrepancy between simulation and measurement is marginal. It can be caused by various effects, including variations of process parameters. Measurement results assuming the calibration injection capacitors being 10% below designed value are added for illustration (solid blue line).

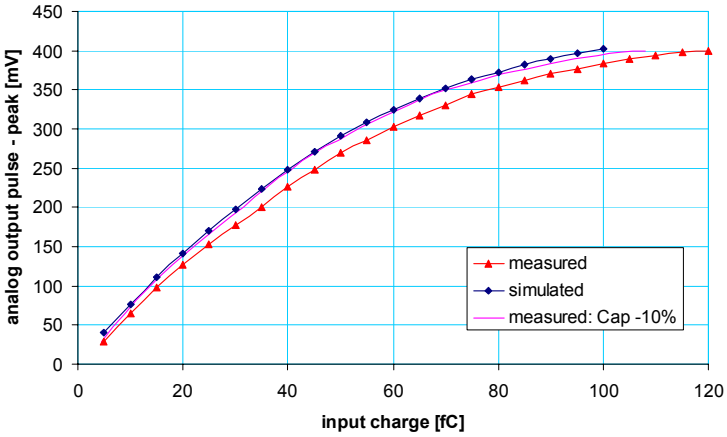


Figure 35. Simulated and measured analog output pulse peak versus input charge using the calibration injection system. The blue solid line represents measurement results assuming the on-chip calibration capacitors being 10% lower than their designed value.

4.1.2 Bipolar shaper

Figure 36 shows a scope picture of the shaper output pulse and its integral. The shaper achieves area balance after ~ 400 ns.

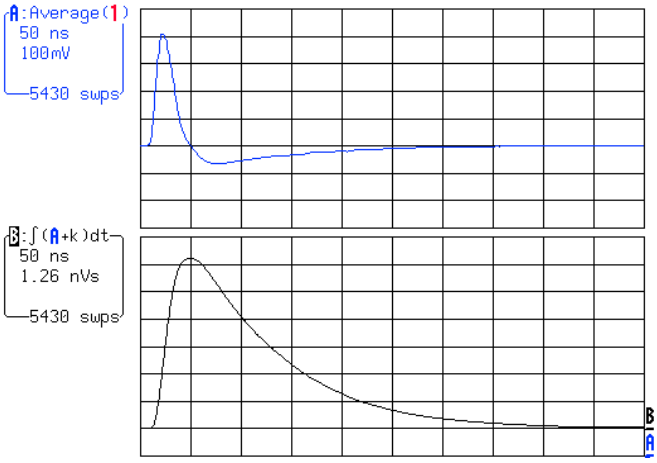


Figure 36. Shaper signal and integral

[5] Although ASD99b does not contain the final functionality (charge ADC, programmability, etc.) it meets all analog specifications.

4.1.3 Analog signal chain sensitivity

Figure 38 shows oscilloscope traces of the shaper output at the threshold coupling point. The measurements were taken with a calibrated probe using well defined input charges. The peaking time (between the arrows) is 14.4 ns. There is a probe attenuation of 10:1 which is not accounted for in the peak voltage values in the left hand column. Due to the differential architecture, the voltages have to be multiplied by a factor 2 to obtain the total gain.

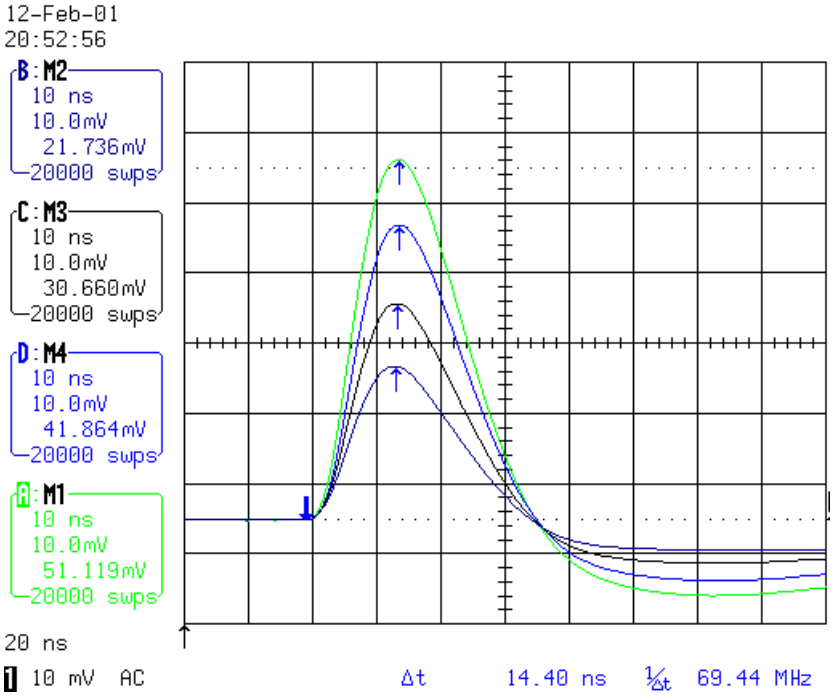


Figure 37. Shaper output for 40, 60, 80 and 100 fC input charge. The peak voltages translate into the sensitivity curve below (Figure 37) by multiplying with a factor of two (single-ended to differential) and including a probe attenuation of 10:1.

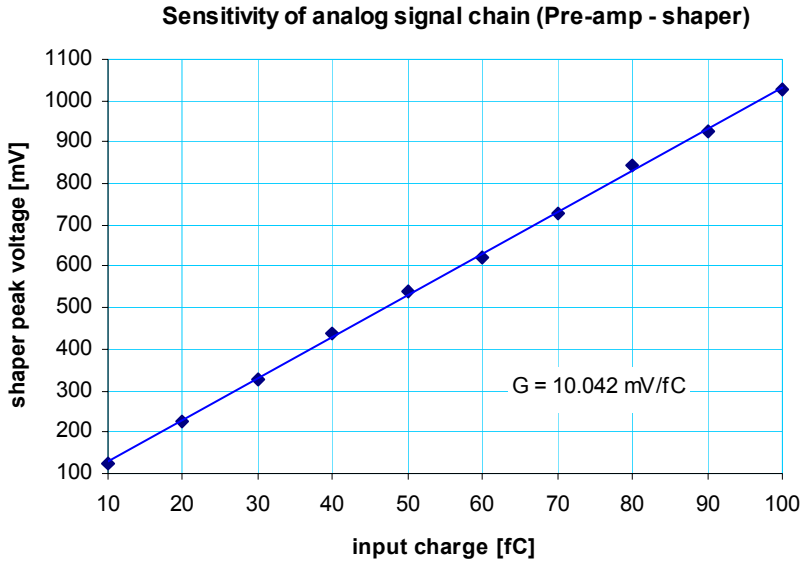


Figure 38. Sensitivity of the analog signal chain (Pre-amp to shaper) for the expected input signal range. The gain amounts to ~ 10 mV/fC, exhibiting very good linearity.

4.1.4 Discriminator time slew

Due to the finite rise time of the signal at the discriminator input, different signal amplitudes with respect to the threshold level produce different threshold crossing times. This effect is called time slew. Figure 39 shows the time slew as measured for a constant threshold by varying the input charge and for a constant input signal by scanning the threshold. The time slew in the expected charge region (~ 20 – 80 fC) is of the order 2 – 3 ns (left plot). The threshold scan of a relatively small signal (27 fC) shows the shape of the leading edge with the 15 ns peaking time (right plot).

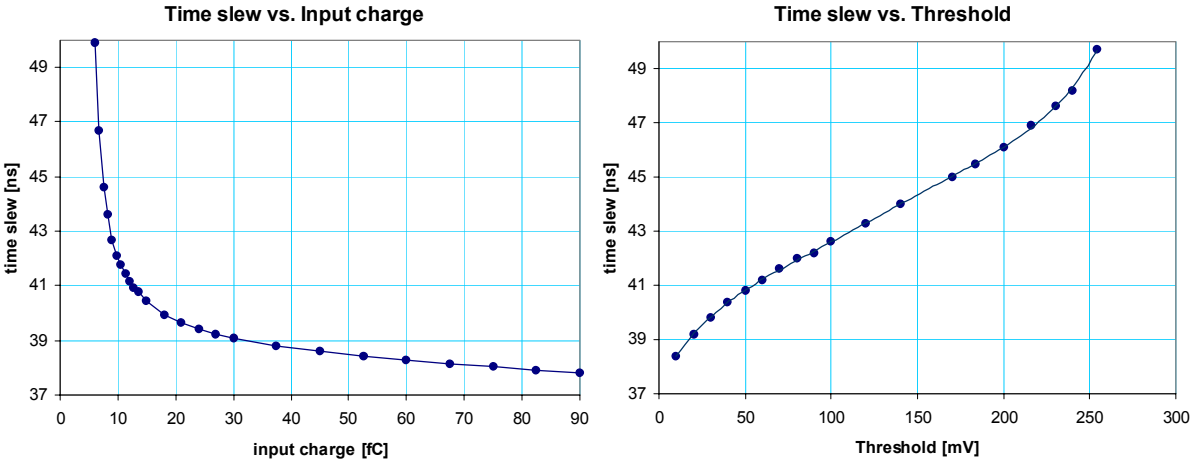


Figure 39. Time slew of the MDT-ASD signal chain. The slew is the timing of the discriminator 50% point of transition as a function of input signal amplitude (left) for a 20 mV threshold and as a function of the threshold (right) for a 27 fC input signal.

4.1.5 Wilkinson ADC performance

The response of the Wilkinson charge ADC as a function of the input charge is shown in Figure 40. The left hand side plot shows the non-linear relation between input charge and output pulse width for 4 different integration gates plotted on a logarithmic scale. The plot on the right hand side shows the sigma of the output pulse width as a function of the input signal. The second data series is again the output pulse width; the integration gate is 15 ns, the scale is linear. As expected, the noise decreases rapidly as the signal starts exceeding the discriminator threshold significantly.

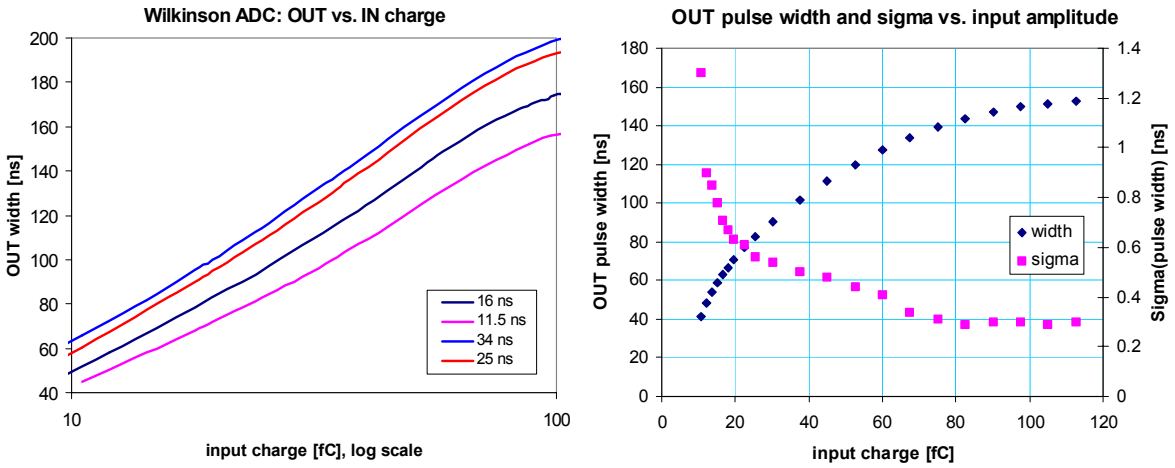


Figure 40. Width of the Wilkinson ADC output pulse as a function of input charge for 4 different integration gate widths (left) on a logarithmic scale. The right plot shows the output pulse width (on a linear scale) and the sigma of the width also as a function of the input signal.

4.1.6 Timing discriminator threshold DAC

Table 9 summarizes the main design parameters and measurement results of the voltage DAC. The characteristic transfer curve is shown in Figure 41. Differential and integral non-linearity, the most important DC performance parameters of a converter, are defined in Table 9 and plotted in Figure 42 and Figure 43.

Table 9. Comparison of specified and measured threshold DAC properties

Parameter	Definition	Specified	Measured	Units
Type	VDAC	–	–	–
Range	$V_{RP} - V_{RN}$	256	256	mV
Resolution	N bits	8	–	–
LSB	$(V_{RP} - V_{RN})/2^N$	1	1	mV
Differential non-linearity	$MAX(V_{n+1} - V_n) - LSB$	< 1	0.7	mV
Integral non-linearity	$MAX(V_n - V_{n,ideal})$	< 5	3.2	mV
Monotonicity	$V_n \leq V_{n+1}\ \forall\ n$	√	√	–
No Missing code	$V_n \neq V_{n+i}\ \forall\ n, i$	√	√	–

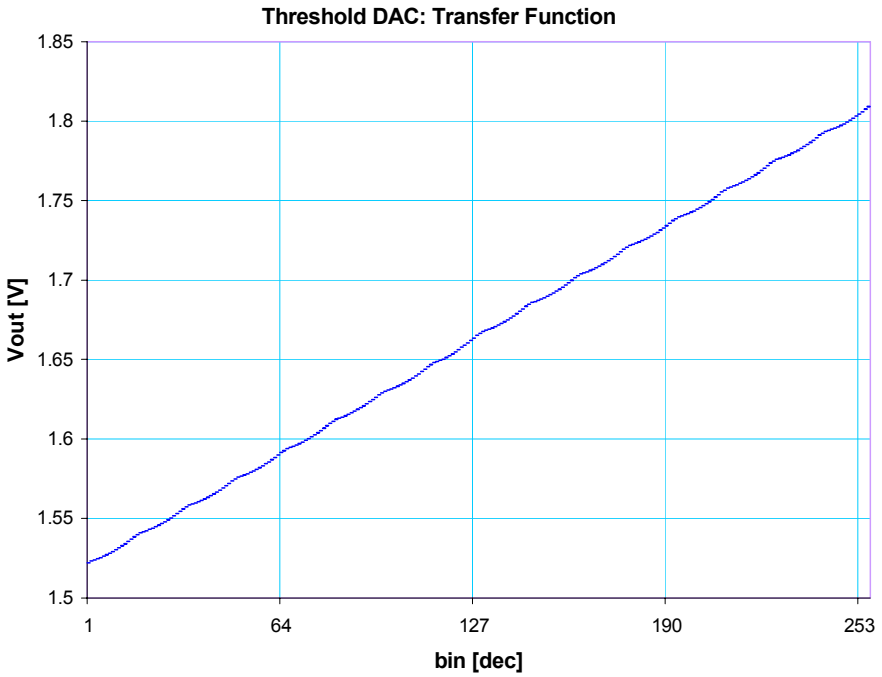


Figure 41. VDAC transfer function

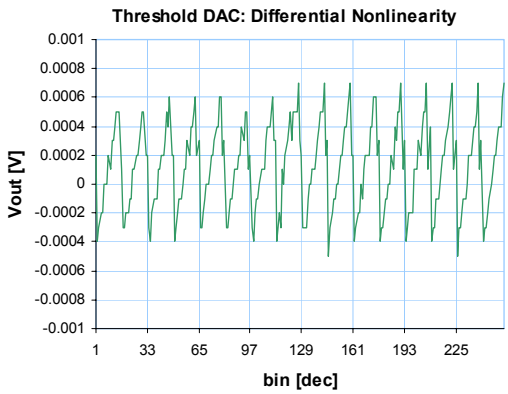


Figure 42. VDAC differential non-linearity

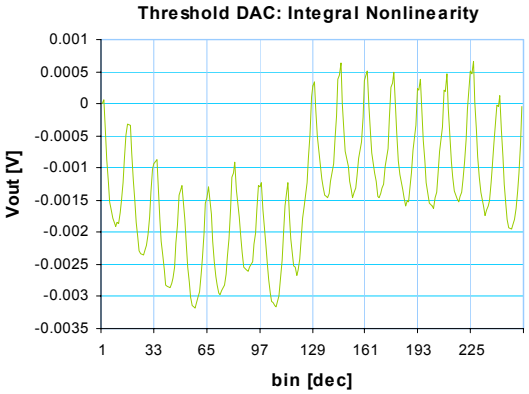


Figure 43. VDAC integral non-linearity

4.1.7 Timing discriminator hysteresis DAC

Hysteresis is applied to the discriminator via a scaled transistor current source DAC. Figure 44 shows the transfer characteristic and the integral non-linearity of the DAC. The maximum integral non-linearity amounts to ±2.5 µA with an LSB of 33 µA.

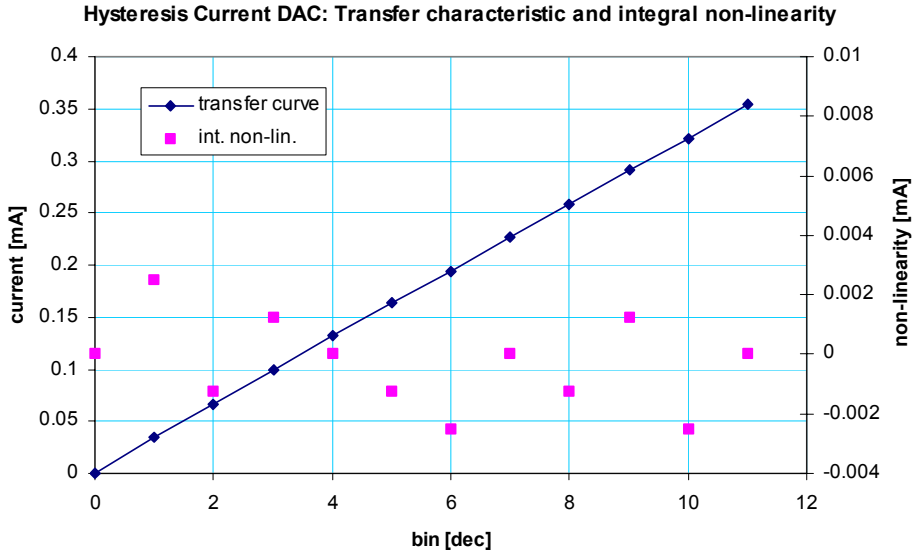


Figure 44. Hysteresis DAC transfer curve and integral non-linearity.

4.1.8 Serial data interface

Tests on the control data interface showed full functionality according to the specifications. The data interface was tested up to a clock frequency of 150 MHz. No data corruption was observed. Registers and logic were tested to work within a supply voltage range of 2.0 V to 5.0 V.

4.1.9 Power consumption

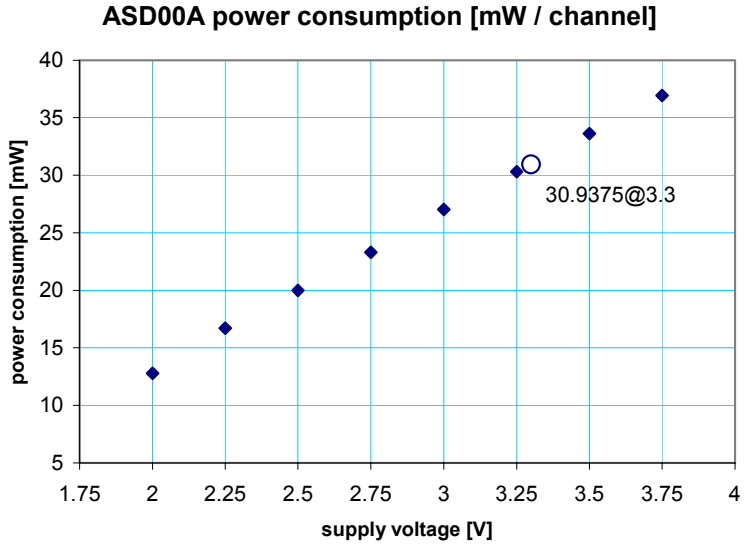


Figure 45. Power consumption versus supply voltage for one channel of the octal ASD00A prototype. The consumption is ~ 31 mW / channel which is in good accordance with the simulated value and slightly below specification (33 mW).

5 Appendix

5.1 MOS transistor models

```
.MODEL CMOSN NMOS                                   LEVEL    = 49
+VERSION = 3.1           TNOM     = 27              TOX      = 9.6E-9
+XJ      = 1.5E-7        NCH      = 1.7E17          VTH0     = 0.6607278
+K1      = 0.7328155     K2       = -0.0164557      K3       = 37.6307825
+K3B     = -0.6826036    W0       = 5.954482E-6     NLX      = 1.160795E-8
+DVT0W   = 0             DVT1W    = 0               DVT2W    = 0
+DVT0    = 5.9023096     DVT1     = 1.0356475       DVT2     = -0.1928577
+U0      = 494.1066594   UA       = 5.793483E-10    UB       = 1.282667E-18
+UC      = 3.434774E-11  VSAT     = 1.259976E5      A0       = 0.9390877
+AGS     = 0.1848153     B0       = 2.222029E-6     B1       = 5E-6
+KETA    = -1.711114E-3  A1       = 0               A2       = 1
+RDSW    = 1.640042E3    PRWG     = -0.0418215      PRWB     = -0.0750653
+WR      = 1             WINT     = 2.612312E-7     LINT     = 1.114883E-7
+XL      = -1E-7         XW       = 0               DWG      = -1.070966E-8
+DWB     = 1.235807E-8   VOFF     = -0.0896698      NFACTOR  = 1.2143784
+CIT     = 0             CDSC     = 1.171765E-4     CDSCD    = 1E-3
+CDSCB   = 2.979369E-5   ETA0     = 1.712692E-3     ETAB     = 3.4153E-3
+DSUB    = 0.7387012     PCLM     = 0.6279545       PDIBLC1  = 0.0416968
+PDIBLC2 = 3.027171E-3   PDIBLCB  = -0.1            DROUT    = 0.4026747
+PSCBE1  = 3.664597E10   PSCBE2   = 1.6701E-8       PVAG     = 0.1613363
+DELTA   = 0.01          MOBMOD   = 1               PRT      = 0
+UTE     = -1.5          KT1      = -0.11           KT1L     = 0
+KT2     = 0.022         UA1      = 4.31E-9         UB1      = -7.61E-18
+UC1     = -5.6E-11      AT       = 3.3E4           WL       = 0
+WLN     = 1             WW       = -1.245E-15      WWN      = 1.125
+WWL     = 0             LL       = 0               LLN      = 1
+LW      = 0             LWN      = 1               LWL      = 0
+CAPMOD  = 2             XPART    = 0.4             CGDO     = 2.51E-10
+CGSO    = 2.51E-10      CGBO     = 1E-11           CJ       = 5.06534E-4
+PB      = 0.99          MJ       = 0.7315511       CJSW     = 4.076138E-10
+PBSW    = 0.99          MJSW     = 0.1             PVTH0    = 3.611855E-4
+PRDSW   = -47.8578499   PK2      = 8.209074E-3     WKETA    = -5.880416E-3
+LKETA   = 1.690549E-3   PAGS     = 0.0968
*

.MODEL CMOSP PMOS                                   LEVEL    = 49
+VERSION = 3.1           TNOM     = 27              TOX      = 9.6E-9
+XJ      = 1.5E-7        NCH      = 1.7E17          VTH0     = -0.8451175
+K1      = 0.374455      K2       = 0.0214736       K3       = 44.5726978
+K3B     = -1.4496401    W0       = 5.256776E-6     NLX      = 8.640935E-8
+DVT0W   = 0             DVT1W    = 0               DVT2W    = 0
+DVT0    = 3.8393012     DVT1     = 0.6051434       DVT2     = -0.0821732
+U0      = 179.9725329   UA       = 1.189439E-9     UB       = 1.189025E-18
+UC      = -5.01386E-11  VSAT     = 1.831276E5      A0       = 0.6676752
+AGS     = 0.325462      B0       = 5.720667E-6     B1       = 5E-6
+KETA    = 9.806091E-4   A1       = 0               A2       = 1
+RDSW    = 2.476373E3    PRWG     = -0.0212227      PRWB     = -0.0823133
+WR      = 1             WINT     = 2.441032E-7     LINT     = 4.330033E-8
+XL      = -1E-7         XW       = 0               DWG      = -2.061704E-8
+DWB     = 1.11758E-8    VOFF     = -0.0956807      NFACTOR  = 0.9637884
+CIT     = 0             CDSC     = 5.707153E-4     CDSCD    = 2.363737E-4
+CDSCB   = 1E-3          ETA0     = 0.0694365       ETAB     = 5.461067E-3
+DSUB    = 0.3174305     PCLM     = 5.4525904       PDIBLC1  = 1.491356E-4
+PDIBLC2 = 4.327953E-3   PDIBLCB  = 0.0181933       DROUT    = 9.994143E-4
+PSCBE1  = 1.235096E10   PSCBE2   = 5.001074E-10    PVAG     = 14.9833684
+DELTA   = 0.01          MOBMOD   = 1               PRT      = 0
+UTE     = -1.5          KT1      = -0.11           KT1L     = 0
+KT2     = 0.022         UA1      = 4.31E-9         UB1      = -7.61E-18
+UC1     = -5.6E-11      AT       = 3.3E4           WL       = 0
+WLN     = 1             WW       = -1.245E-15      WWN      = 1.025
+WWL     = 0             LL       = 0               LLN      = 1
    +LW      = 0             LWN      = 1               LWL      = 0
+CAPMOD  = 2             XPART    = 0.4             CGDO     = 2.44E-10
+CGSO    = 2.44E-10      CGBO     = 1E-11           CJ       = 9.335184E-4
+PB      = 0.9260485     MJ       = 0.4724799       CJSW     = 1.466932E-10
+PBSW    = 0.4542609     MJSW     = 0.1167867       PVTH0    = 5.089527E-3

+PRDSW   = 37.6262554    PK2      = 2.784938E-3     WKETA    = 4.449153E-3
+LKETA   = -2.10717E-3   PAGS     = 0.12532
*
```

5.2 LVDS driver properties

The characteristics of the MDT-ASD LVDS-drivers on an ASD99D were assessed according to the specifications in the IEEE P1596.3 (LVDS) standard document.

5.2.1 Driver DC specifications

Table 10 gives the LVDS "reduced range link" driver DC specifications for a nominal 100 Ω termination and results from measurements at a power supply voltage of 3.3 V. All measurement results lie within the specifications at nominal conditions.

Table 10. LVDS "reduced range link": Driver DC specifications and ASD LVDS driver properties measured at V_{sup}= 3.3V

Symb.	Parameter	Conditions	Min	Max	Meas	Unit
V_{oh}	Output voltage high, V_{oa} or V_{ob}	R_{load} = 100 Ω ± 1%		1375	1335	mV
V_{ol}	Output voltage low, V_{oa} or V_{ob}	R_{load} = 100 Ω ± 1%	1025		1165	mV
$\|V_{od}\|$	Output differential voltage	R_{load} = 100 Ω ± 1%	150	250	170	mV
V_{os}	Output offset voltage	R_{load} = 100 Ω ± 1%	1150	1250	1250	mV
R_0	Output impedance, single ended	V_{cm} = 1.0V and 1.4V	40	140	-	Ω
ΔR_0	R_0 mismatch between a & b	V_{cm} = 1.0V and 1.4V		10	-	%
$\|\Delta V_{od}\|$	Change in $\|V_{od}\|$ between `0` and `1`	R_{load} = 100 Ω ± 1%		25	2	mV
ΔV_{os}	Change in V_{os} between `0` and `1`	R_{load} = 100 Ω ± 1%		25	1	mV
I_{sa}, I_{sb}	Output current	Driver shorted to ground		40	3.7	mA
I_{sab}	Output current	Drivers shorted together		12	1.5	mA

Figure 46 shows the variation of the driver dc levels as a function of the power supply voltage VDD. The upper voltage level V_{oh} remains below the specified maximum up to a VDD of 3.42 V. The lower voltage level V_{ol} remains above the specified minimum down to a VDD of 2.9 V. The output offset voltage V_{os} stays within the specified range for a VDD between 3.0 V and 3.3 V.

Figure 47 shows the dependency of the driver output differential voltage V_{od} on the power supply voltage VDD. V_{od} lies within the specified range from VDD = 3.17 V to VDD well above 3.6 V.

Driver DC levels are measured to lie within the LVDS reduced range link standard specification for a power supply voltage variation from **3.17 V to 3.3 V (VDD_{nom} - 4% to VDD_{nom} + 0%) at nominal termination (100 Ω).**

Figure 48 and Figure 49 show the variation of the driver dc levels as a function of the power supply voltage for a termination resistance R_{load} = 200 Ω, V_{oh} exceeds the upper limit at VDD = 3.22 V, V_{os} stays in range from 3 V to 3.44 V, V_{ol} from 3.05 V upwards.

The variation of the driver output differential voltage V_{od} as a function of load resistance is shown in Figure 50. V_{od} remains within the specified limits for R_{load} from 90 Ω to 150 Ω at VDD = 3.3 V.

ΔV_{os}, the change in output offset voltage between `0` and `1` is shown in the bottom oscilloscope trace of Figure 51. V_{oa} and V_{ob} are represented by the top traces labeled 1 and 2. The amplitude cursor yields a difference of 2 mV. This number has to be divided by 2 according to $V_{os} = (V_{oa} + V_{ob})/2$, yielding the value of 1 mV in Table 10.

$|\Delta V_{od}|$ was measured in a similar way (compare Figure 54).
The short-circuit output currents I_{sa}, I_{sb} and I_{sab} were measured according to the definitions in the LVDS standard document.

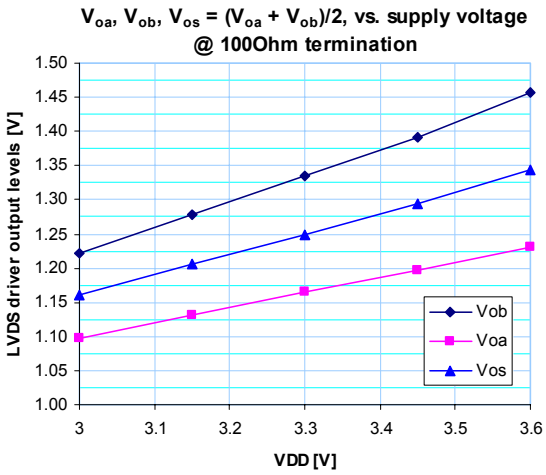


Figure 46. Driver DC levels V_{oa}, V_{ob}, V_{os} vs. supply voltage at nominal load (100 Ω)

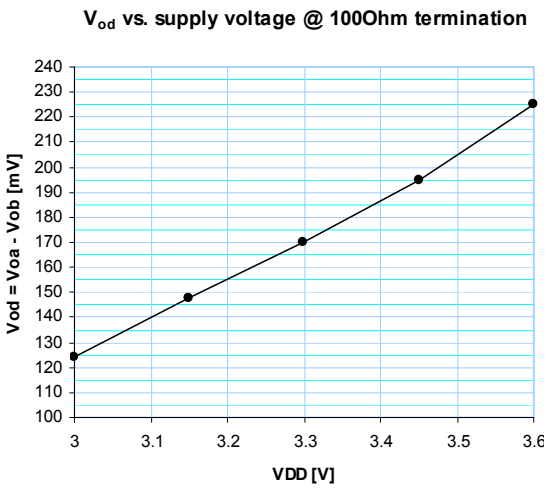


Figure 47. Driver differential voltage V_{od} vs. supply voltage at nominal load (100 Ω)

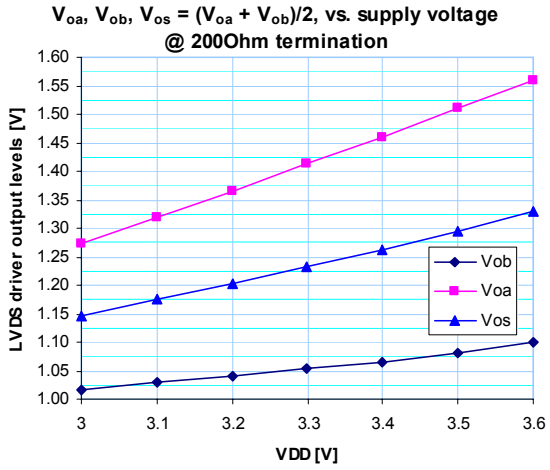


Figure 48. Driver DC levels V_{oa}, V_{ob}, V_{os} vs. supply voltage at 200 Ω load

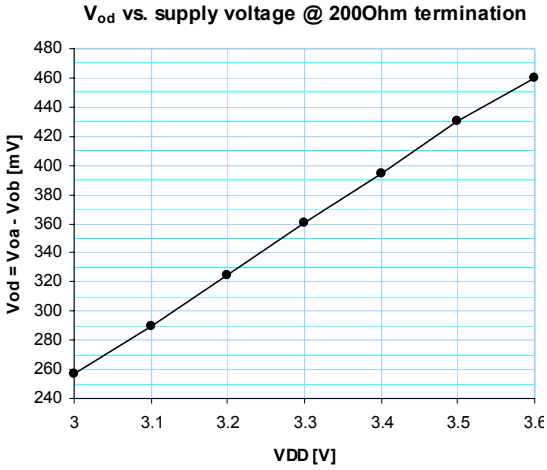


Figure 49. Driver differential voltage vs. supply voltage at 200 Ω load

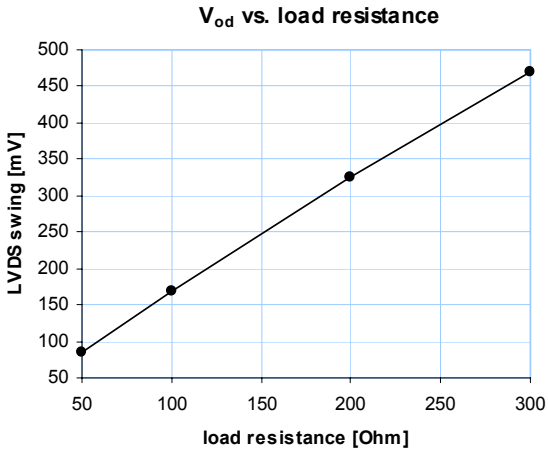


Figure 50. Driver differential voltage vs. load resistance

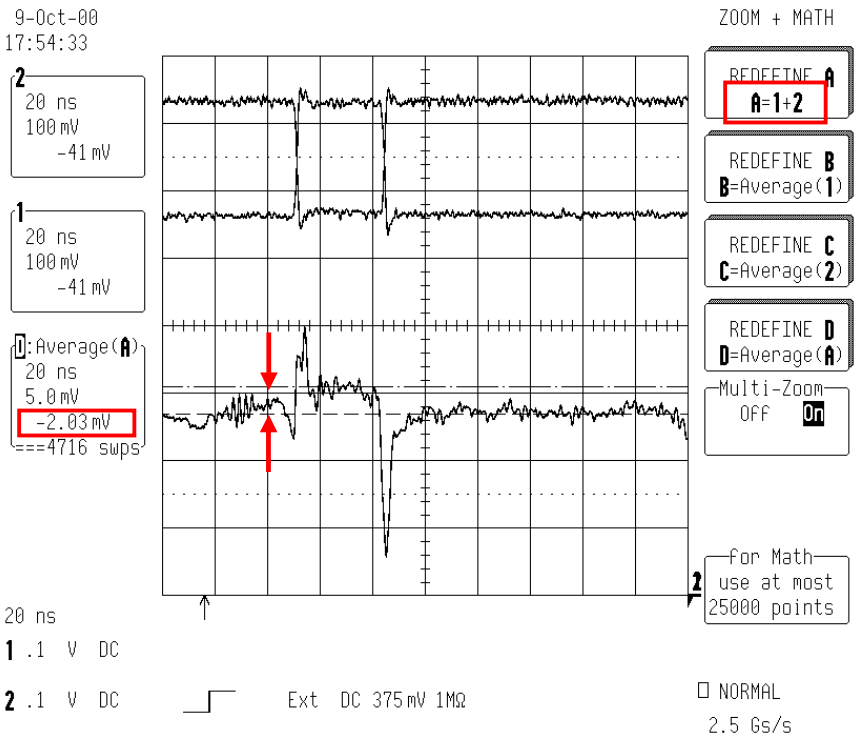


Figure 51. ΔV_{os} - change in output offset voltage V_{os} between `0` and `1`

5.2.2 Driver AC specifications

The LVDS standard document specifies AC parameters for clock and data signals. Relevant for MDT-ASD are rise- and fall-time and differential skew, while clock signal duty cycle and channel-to-channel skew are not applicable. Table 11 gives the LVDS driver AC specifications for a nominal 100 Ω termination and results from measurements at a power supply voltage of 3.3 V. Rise- and fall-time (Figure 53) exceed the specifications by a factor of 2, skew (Figure 55) lies well within specs. The measurements were done under conditions illustrated in Figure 52.

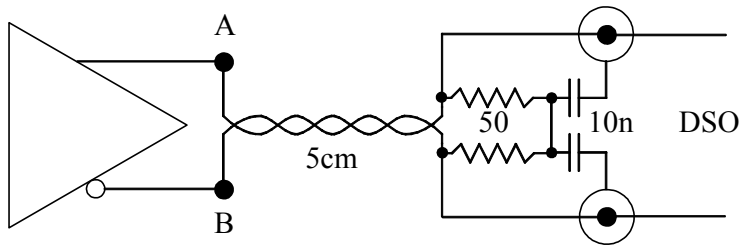


Figure 52. Connection setup: 5cm twisted pair terminated with 50 Ω resistors, 10nF caps to scope ground.

Table 11. LVDS Driver AC specifications and MDT-ASD LVDS driver properties measured at V_{sup}= 3.3 V

Symbol	Parameter	Conditions	Min	Max	Meas	Unit
t_{fall}	V_{od} fall time, 20% to 80%	Z_{load} = 100 Ω ± 1%	300	500	940	ps
t_{rise}	V_{od} rise time, 20% to 80%	Z_{load} = 100 Ω ± 1%	300	500	970	ps
t_{skew}	Differential skew $\|tp_{HLA} - tp_{HLB}\|$ or $\|tp_{HLB} - tp_{HLA}\|$	Any differential pair, @ 50% point of transition		50	20	ps

Measurements in Figure 53 and Figure 54 were taken at a test pulse frequency of 25 MHz. No high rate effects were observed. Figure 53 gives rise- and fall-times t_{rise} and t_{fall}, the output differential voltage V_{od} and the output offset voltage V_{os}. Figure 54. yields $|\Delta V_{od}|$.

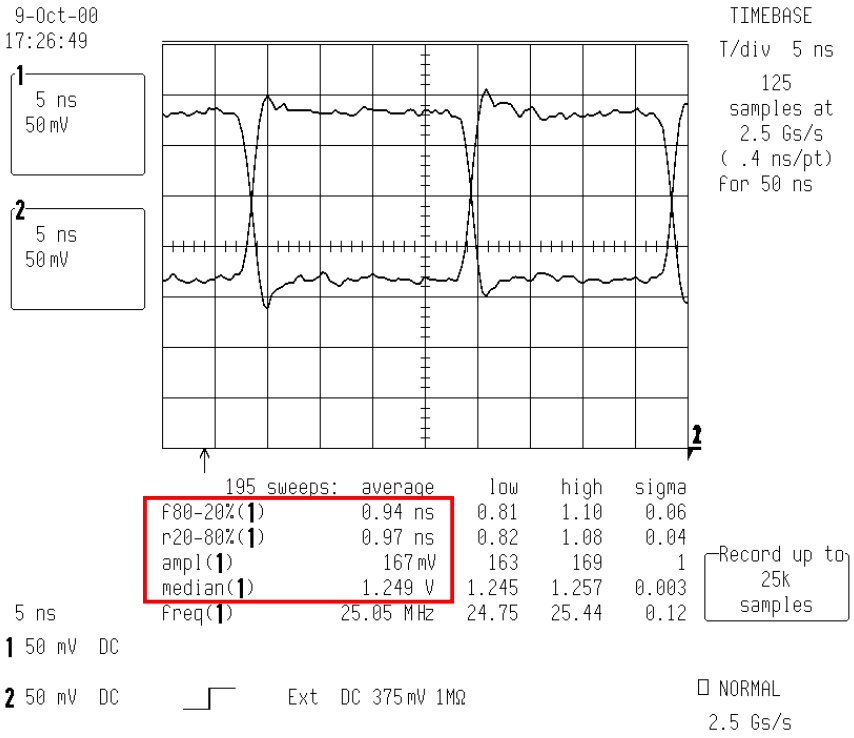


Figure 53. t_{rise} and t_{fall}, V_{od} = ampl(1), V_{os} = median(1)

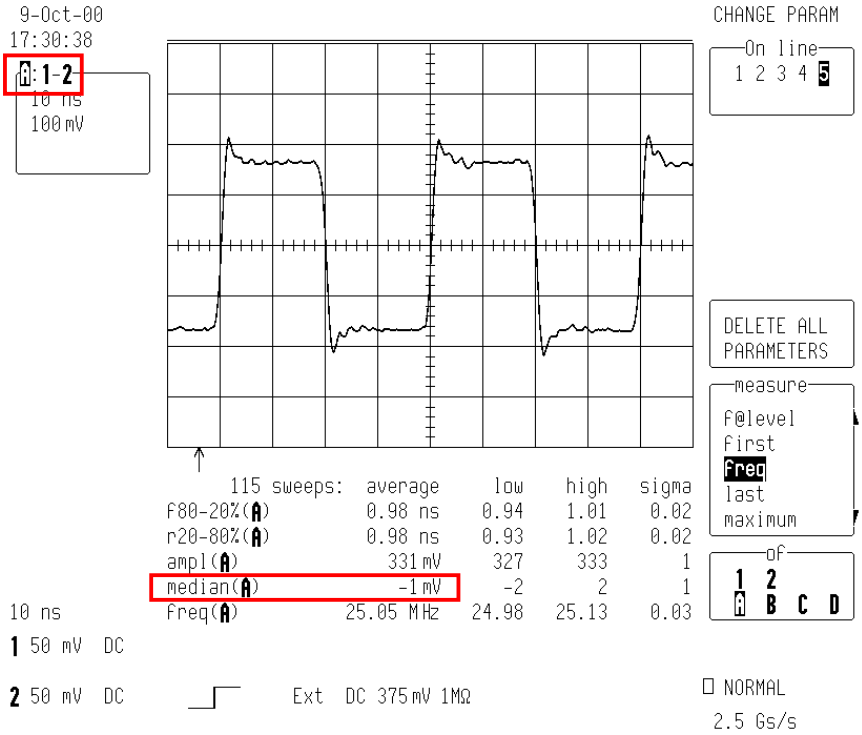


Figure 54. $|\Delta V_{od}|$ = 2 |median(A)| = 2 mV

The skew measured in Figure 55 is the time difference between the high-to-low and low-to-high transitions of complementary single ended channels measured at the 50% level. The measured value of 20 ps is well below the specified maximum of 50 ps.

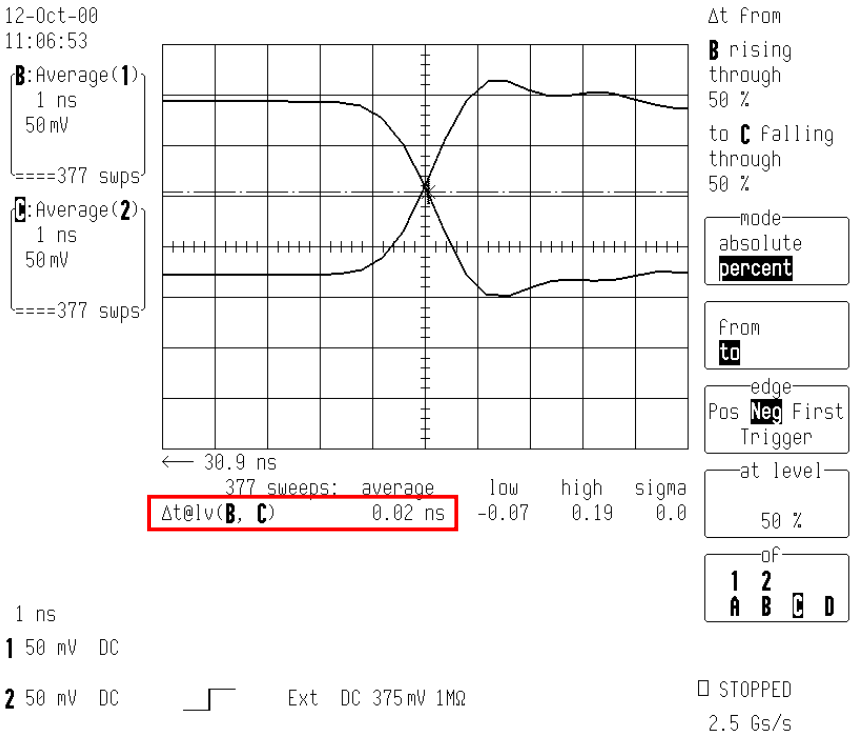


Figure 55. Skew - time difference between the high-to-low and low-to-high transitions measured at 50%: 20 ps

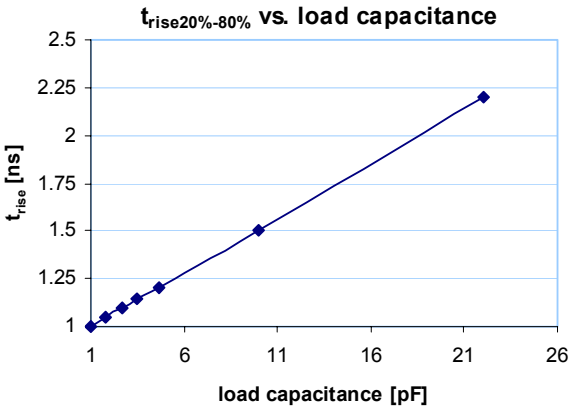


Figure 56. t_{rise} vs. load capacitance

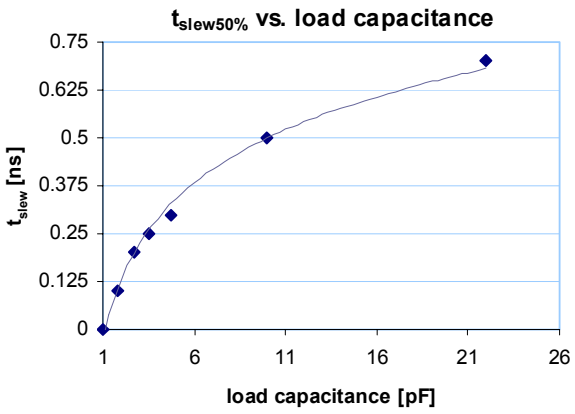
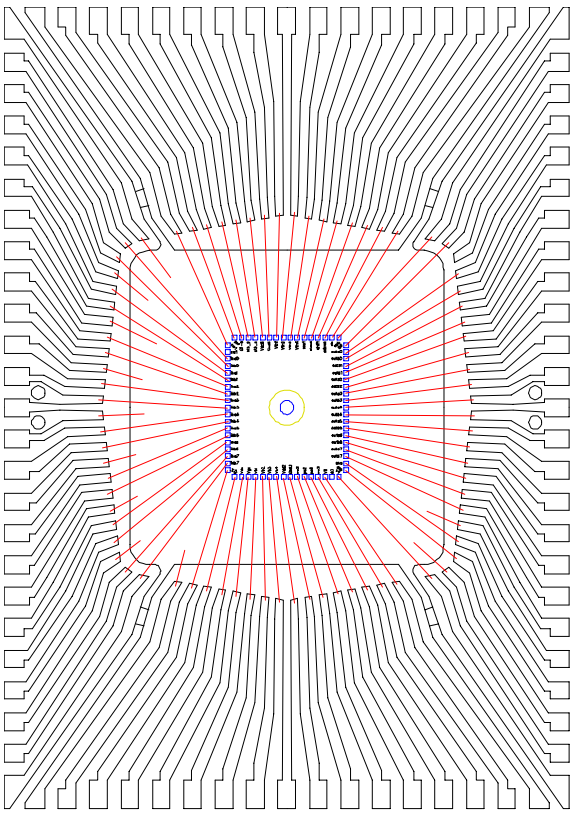


Figure 57. $t_{slew50\%}$ vs. load capacitance

Figure 56 shows the increase of t_{rise} as a function of the load capacitance. Time slew measured at V_{os} versus load capacitance is shown in Figure 57.

Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE P1596.3-1995 standard document.

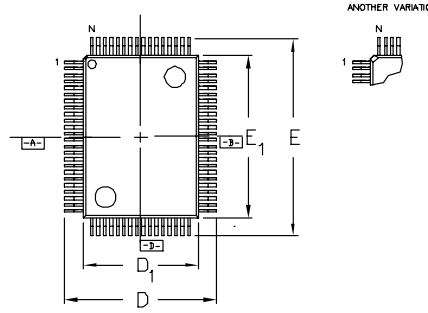
5.3 Packaging information



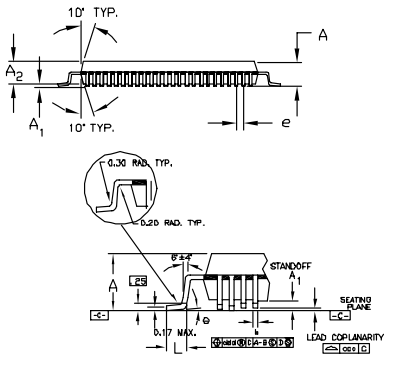
ASAT

REVISIONS				
ECN	REV	DESCRIPTION	DATE	APPROV
S0650	A	NEW DRAWING	9/26/95	
S0685	B	ADD MAX. STANDOFF IN 2.7 BODY THICKNESS.	6/20/96	
S0719	C	CHANGE 64L & DIM. TO .484+/-.004	9/17/96	

ANOTHER VARIATION OF PIN 1 VISUAL AID



2.70 mm THICK, BODY + 3.2 mm / BODY + 3.9 mm FOOTPRINT						
DIMS.	TOLS. / LEADS	64L	80L	100L	120L	128L
A	MAX.	3.40				
A_1	MIN./MAX.	.25/.50				
A_2	±.10	2.70				
D	±.20	17.20 / 17.90				
D_1	±.10	14.00				
E	±.20	23.20 / 23.90				
E_1	±.10	20.00				
L	+.15/−.10	.88				
e	BASIC	1.00	.80	.65	.50	
b	±.05	.40	.35	.30	.22	
θ		0°–7°				
ddd		.20 NOM.	.20 NOM.	.12 NOM.	.08 MAX.	
ccc	MAX.	.10			.08	



2.00 mm THICK, BODY + 3.2 mm FOOTPRINT						
DIMS.	TOLS. / LEADS	64L	80L	100L	120L	128L
A	MAX.	2.35				
A_1	MAX.	.25				
A_2	±.10	2.00				
D	±.20	17.20				
D_1	±.10	14.00				
E	±.20	23.20				
E_1	±.10	20.00				
L	+.15/−.10	.88				
e	BASIC	1.00	.80	.65	.50	
b	±.05	.40	.35	.30	.22	
θ		0°–7°				
ddd		.20 NOM.	.20 NOM.	.12 NOM.	.08 MAX.	
ccc	MAX.	.10			.08	

NOTES : 1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOLERANCES AS INDICATED.
3) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, 0.25 ABOVE THE SEATING PLANE.

ASAT Inc.			
DRAWN AH-SAN	14x20 mm QFP MARKETING OUTLINE		
DATE 9/17/96			
CHECKED NIC B.	DRWG NO. DGMQ14201	REV C	SHEET 1/

6 References

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