

# **Preliminary Design Review of the MDT Electronics**

## **(TDC part)**

Review Date : Feb. 22, 2001

Yasuo Arai

KEK, National High Energy Accelerator Research Organization

Institute of Particle and Nuclear Studies

yasuo.arai@kek.jp, <http://www-atlas.kek.jp/~arai/>

# Contents

<b>1. INTRODUCTION</b>	<b>3</b>
<b>2. REQUIREMENTS</b>	<b>3</b>
<b>3. SPECIFICATIONS</b>	<b>7</b>
<b>4. ARCHITECTURE</b>	<b>8</b>
4.1 Fine Time Measurement	9
4.2 Coarse Counter	10
4.3 Channel Buffer.	10
4.4 Encoder	11
4.5 L1 Buffer.	11
4.6 Trigger Matching.	12
4.7 Trigger Interface.	13
4.8 Encoded trigger and resets signal	13
4.9 Read-out FIFO.	13
4.10 Serial Readout	14
4.11 Packet format	15
4.12 Error monitoring.	15
4.13 JTAG Port.	16
4.14 CSR Registers	17
<b>5. SIMULATION STUDY</b>	<b>18</b>
5.1 Hit and trigger generation	18
5.2 Channel buffer occupancy	19
5.3 First level buffer occupancy	19
5.4 Trigger Search time	20
5.5 Trigger FIFO occupancy	20
5.6 Readout Buffer occupancy	21
<b>6. PROTOTYPE PERFORMANCE</b>	<b>21</b>
6.1 PLL and Ring Oscillator	22
6.2 Channel Buffer	23
6.3 Time Resolution and Non-Linearity	25
6.4 Power Consumption	26
6.5 TDC IRRADIATION TEST	26
<b>7. REMAINING DEVELOPMENTS</b>	<b>28</b>
7.1 Low Power LVDS receiver	29
7.2 JTAG control circuit for the ASD	31
<b>8. SCHEDULE</b>	<b>31</b>
<b>9. REFERENCES</b>	<b>31</b>

## 1. Introduction

A TDC with sub-nano second resolution is required to obtain the necessary spatial resolution of the Monitored Drift Tubes (MDT). It must be capable of measuring closely spaced pulses without introducing any additional dead time. The high rates expected in the ATLAS detector requires that the TDC is capable of continuously accepting new hits while selectively extracting hits related to a trigger after the first level trigger latency. To do this several levels of data buffering is required to keep up with the trigger rates and hit rates expected in the experiment.

The TDC is named AMT (ATLAS Muon TDC). Basic requirements on the AMT chip were summarized in ATLAS note (MUON-NO-179, May 1997) [1] and presented at LEB97[2]. Then AMT-0 [3] was designed in a 0.7  $\mu\text{m}$  full custom CMOS process based on the 32 channel TDC for the quick test of front-end electronics and MDT chambers.

On the other hand, it was decided to use a Toshiba's 0.3  $\mu\text{m}$  CMOS process for a final production. To develop and test many critical elements in the 0.3  $\mu\text{m}$  process, a TEG (Test Element Group) chip (AMT-TEG) was designed, fabricated and tested successfully at KEK [4, 5]. Then AMT-1 chip was developed in which all essential requirements were implemented and successfully tested, and it is now used for 10k channel test of MDT detector and electronics.

Next version of AMT chip (AMT-2) is now under development, which fix several minor bugs and increase testability. Furthermore, a JTAG control circuit for the ASD and a new low-power LVDS receiver circuit will be implemented in the AMT-2.

## 2. Requirements

Block diagram of the MDT front-end electronics is shown in Fig. 1. Three ASD (Amp-Shaper-Discriminator) chips [6] and one AMT chip are mounted on a small multi-layer printed circuit board (mezzanine board), which plugs into a MDT end plug PCB (signal hedgehog board).

Two modes of operation will be provided in MDT measurement. In one mode the ASD output gives the time over threshold information, i.e. signal leading and trailing edge timing. The other mode measures leading edge time and charge (pulse width). The Wilkinson ADC serves as a time slew correction and also provides diagnostics for monitoring chamber gas gain. It operates by creating a gate of  $\sim 20\text{ns}$  width at the leading edge of the signal, integrating charge onto a holding capacitor during the gate, and then running down the hold capacitor at constant current (the maximum rundown time is of order 200ns). The discriminator also generates artificial dead time to avoid multiple hits.

Requirements to the AMT are described in reference [1] and summarized below.

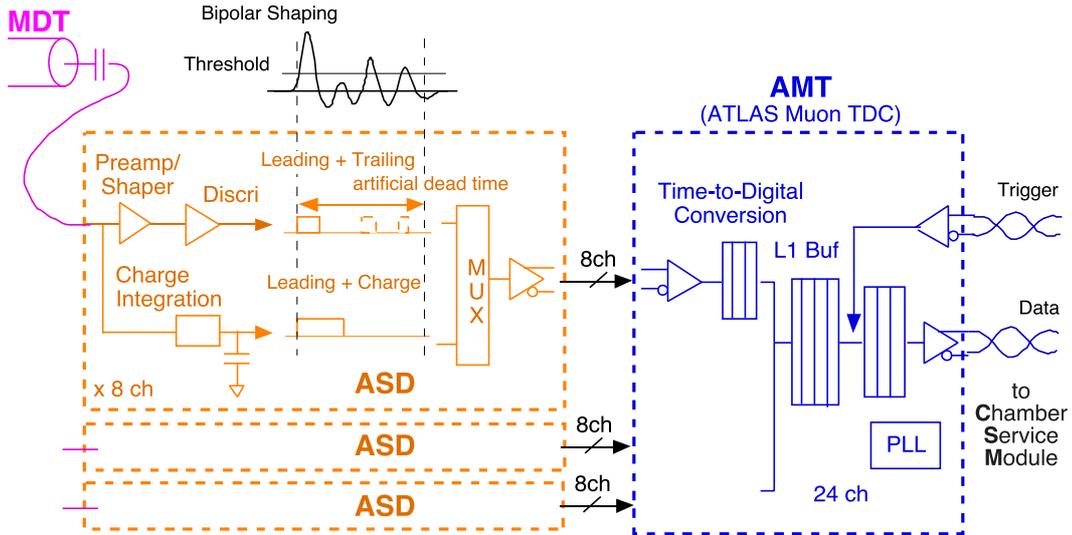


Fig. 1 MDT front-end electronics. AMT chip receives timing signal from three ASD chips and sends data to a Chamber Service Module.

### Time Resolution

To achieve a 60  $\mu\text{m}$  single-tube resolution, a timing resolution of better than 1 ns is required.

### Masked Hits

The signal from a round drift tube has a long tail. A second track might therefore be masked by the signal tail of a preceding track. The existence of a preceding hit can be detected by checking the data before the trigger matching region. This masked hit information can be sent out with one word per event using a flag bit for each channel.

### Hit Rate

The maximum hit rate in a wire is estimated to be 400 kHz at BIS3 (calculated from TP43 simulation [7]) while most of wire has less than 100 kHz hit rate. This number contains factor 5 safety factor and calculated at the  $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  luminosity.

### Drift Time

The maximum drift time of the drift tube is considered less than 800 ns.

### Number of channels

There are about 37,000 MDT tubes in total. Since the number of tube layers is 3 and 4, and the ASD chip will have 8 channels per chip, a 24 channel TDC matches well this configuration.

### Bunch Counter and Coarse Counter

There are 3564 clock periods and 2835 real bunch crossings per LHC beam revolution. Bunch crossings are identified with a 12 bit Bunch Crossing Identifier (BCID) [8]. To correctly identify hits within the bunch structure a 12 bit coarse time counter is required in the TDC.

### TDC Clock

A TDC clock with the same frequency as the bunch crossing rate must be used. In this way the coarse time count can be correlated directly with the bunch count. In some internal parts of the TDC, such as the PLL or the serial interface, a 2 times higher clock frequency is used to improve performance. A high speed clock will in this case be phase locked to the beam clock.

### Trigger Interface

When a trigger signal is given to the first level buffers, measurements related to that event must be extracted from the buffer and sent to the data acquisition system.

Trigger conditions are summarized below;

- maximum level 1 trigger rate is 75 kHz (100 kHz in future upgrade)
- level 1 trigger latency is around 2.5  $\mu$ s
- minimum interval between two triggers is 125 ns
- there are no more than 8 triggers in any given 80  $\mu$ s period.  
(this is not yet officially approved?)

Each event accepted by the first level trigger is identified by a 24 bit event ID at the system level. At the TDC a reduced event ID of 12 bits is used.

### Configuration and Signal levels

It is of vital importance that noise from digital signals on the front-end board is kept to an absolute minimum so the small analog signal from the tubes are not corrupted. LVDS (Low Voltage Differential Signaling, IEEE 1596.3) signals are used for all connections to/from the TDC which are actively running while taking data.

Hit data selected by a trigger must be transferred from the TDC to the CSM (Chamber Service Module) located outside the detector. The distance from the TDCs to the CSM is of the order of 10 meters. The connection from the TDCs to the CSM is performed on serial links of 40 Mbits/s (or 80 Mbits/s)..

### Data Packet

Data packets of 32 bit are used in the serial data stream. The first four bits of the packet are allocated to a type identifier which specifies the type of data. The following four bits are allocated for a TDC chip identifier. This ID is used just for confirmation of the connection. Since maximum number of TDC per chamber is 18, actual TDC ID is added to data at the CSM. Event data from different events can be separated by the optional use of a header and a trailer.

A header must contain the event ID and bunch ID of the event being readout. A trailer must contain the event ID and a word count. All required information from a hit: type identifier, TDC ID, channel ID, leading edge time plus pulse width must be contained in one 32 bit word. The conditional mask flags for the 24 TDC channels must also be contained in a single 32 bit word. In case a TDC have detected an internal error condition (e.g. buffer overflow) it must send a special error status package for all events which may have been affected by the error.

### Data Rate

At a 400 kHz hit rate per TDC channel and a trigger matching window of 800 ns, an average of 6 hits per TDC is expected at highest rate locations. For each hit, 35 bits (32 bits data + start bit + stop bit + parity) must be transferred from a TDC to the CSM. With a trigger rate of 100 kHz this requires an average serial bandwidth of 28 Mbits/s per TDC including the header and trailer.

### Serial Link Protocol

A coding scheme of the serial data is the two wire signaling scheme. There are several options for such scheme. One is the DS protocol ( IEEE P1355 ) which keeps the required bandwidth to an absolute minimum. Another one is simple data and clock pair. This requires higher bandwidth in the link but simplify the receiving circuit.

To limit the number of cables in the detector it is not considered to have a back propagation signal from the DAQ to the TDC telling it to stop sending data in case buffers in the DAQ system are running full.

Instead buffer full flag is added to data if the buffer overflow occurs and the TDC must be capable of recovering event synchronization locally without any higher level intervention from the DAQ system.

### System setting and debugging.

The fact that the TDC is going to be embedded inside the detector requires special attention on monitoring and in system testing capabilities. The cause and place of hardware failures must be detectable without opening the detector such that the effect of a hardware failure can be minimized and such that a repair can be performed fast and effectively. A relatively slow bi-directional communication path is also necessary to be capable of loading setup and calibration parameters before data taking and to monitor the system during operation.

The standard IEEE 1149.1 JTAG protocol is used for this purpose. The use of full boundary scan enables efficient testing of TDC module failures while located in the system. Testing the functionality of the chips themselves are also supported by JTAG. To insure fast and effective testing of embedded memory and data path structures in the TDC chip special scan path registers must be implemented for this.

### Radiation tolerance

AMT chip is used at the end of MDT chamber, so the chip must have adequate radiation tolerance. Simulated Radiation Levels for total ionizing doze (SRLtid) is 2.8 Gray/year for worst location MDT at  $10^{34}$  luminosity[9]. Actual Radiation Tolerance Criteria (RTC) is calculated from following equations.

$$RTCTid = SRLtid \cdot SFsim \cdot SFldr \cdot SFlot$$

Here,

SFsim : Represents SRL inaccuracies.

SFldr : Represents low dose rate effects.

SF<sub>lot</sub> : Represents the variation of radiation tolerance from lot to lot and within a lot.

SF<sub>ldr</sub> is '1' if accelerated aging tests at elevated temperature are done. SF<sub>lot</sub> will also be '1' if the chips are produced in one lot. SF<sub>sim</sub> is assumed as '4'. Thus maximum value of the RTCT<sub>id</sub> for 10 years operation is;

$$(RTCT_{id})_{max} = 2.8 \text{ (Gray)} \times 4 \times 1 \times 1 \times 10 \text{ (years)} = 112 \text{ Gray} = 11.2 \text{ krad}$$

NIEL(Non-Ionizing Energy Loss) test on pure CMOS devices is not required from ATLAS, since CMOS devices are naturally tolerant to displacement damage.

Radiation may also introduce single event upsets by accidentally changing the state of a memory element in the TDC. The effect of such an event must be minimized and should be detected by the TDC itself possibly using error detecting/correcting codes in all internal memory structures.

### 3. Specifications

Specification of the AMT chip is summarized in Table. 1.

Table. 1 AMT Specifications

(System Clock Frequency is 40 MHz)

• Least Time Count	0.78 ns/bit (rising edge) 0.78-100ns/bit (falling edge)
• Time Resolution	RMS = 300 ps (rising edge) ? RMS = 300ps ~ 29ns (falling edges)
• Dynamic range	13 + 4 = 17 bit (102.4 μsec)
• Integral Non Linearity	Max = +/-80 ps ?
• Differential Non Linearity	Max = +/- 80 ps ?
• Difference between channels	Maximum one time bin
• Stability	< 0.1 LSB (3.0 - 3.6 V, 0 - 70 °C)
• Input Clock Frequency	10 - 70 MHz (@ x2 mode)
• PLL mode	x2
• Internal System Clock	Input Clock x (PLL mode) / 2
• No. of Channels	24 Channels
• Level 1 Buffer	256 words
• Read-out Buffer	64 words
• Trigger Buffer	8 words
• Double Hit Resolution	<10 ns
• Max. recommended Hit rate	500 kHz per channel
• Hit Input Level	Low Voltage Differential Signaling (LVDS) Internal 100 Ohm termination.
• Supply Voltage	3.3+-0.3V (< 200 mA)
• Temperature range	0 - 85 Deg. Cent
• Process	0.3 μm CMOS Sea-of-Gate (Toshiba TC220G) die size: 6 mm x 6 mm
• Package	0.5 mm lead pitch, 144 pin plastic QFP

## 4. Architecture

Fig. 2 shows a block diagram of the AMT chip.

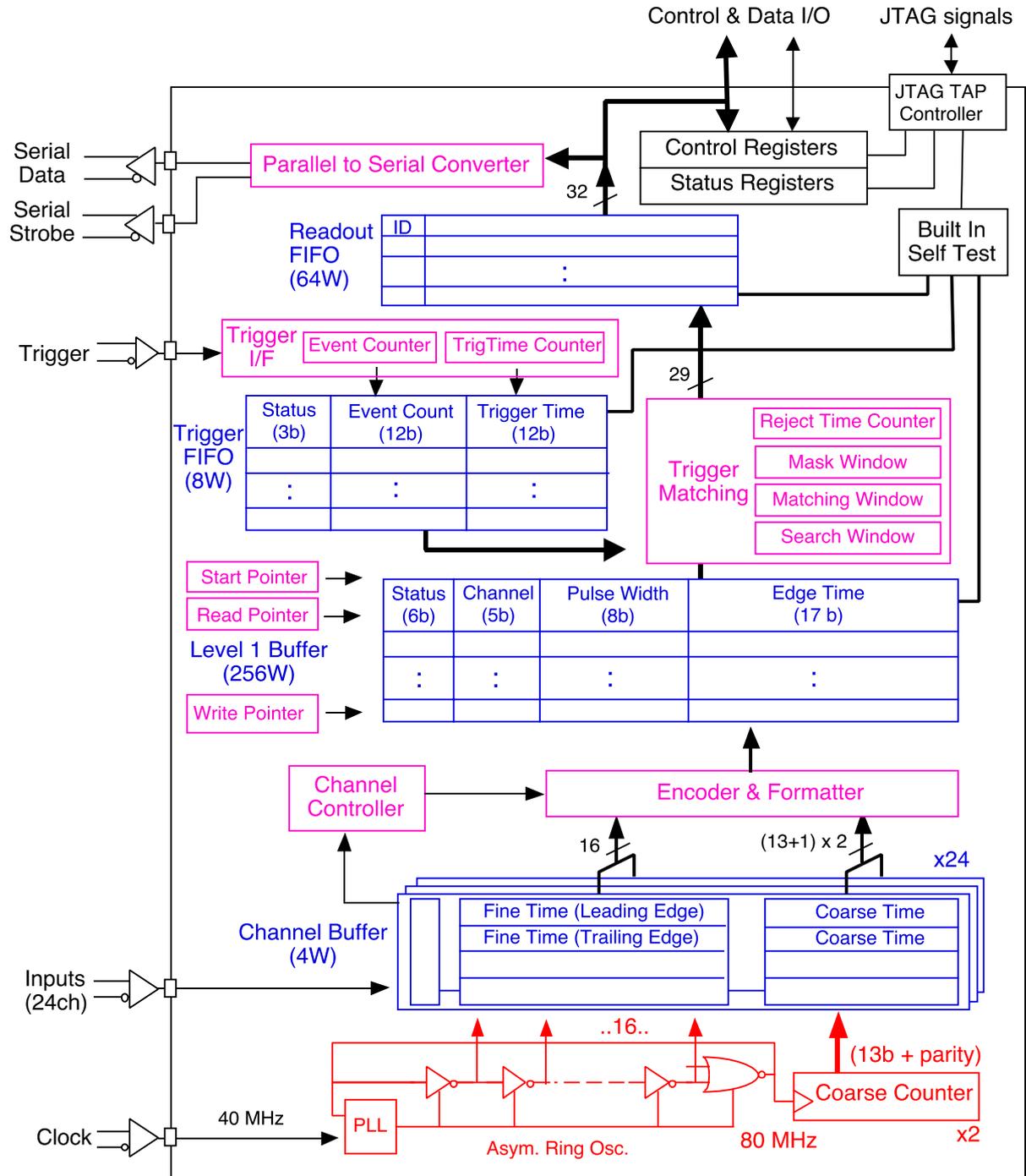


Fig. 2 Block Diagram of the AMT chip.

The hit signal coming from the ASD chip via LVDS is used to store the fine time and coarse time measurement in individual channel buffers. The fine time measurement is obtained from 16 taps of a asymmetric ring oscillator which is stabilized with a Phase Locked Loop (PLL). The timing of both leading and trailing edge of the hit signal can be stored as a pair to enable a pulse width measurement to be performed.

The time measurements from the channel buffers are stored during the first level trigger

latency in a common first level buffer. First level triggers converted into trigger time tags and a corresponding event ID are stored temporarily in a trigger FIFO waiting to be matched with the hit measurements from the first level buffer. Hits matching triggers are written into a readout FIFO waiting to be transferred to the DAQ system via a serial link.

The architecture of the AMT is described in several documents [10, 11] and briefly described below.

#### 4.1 Fine Time Measurement

A new kind of voltage controlled ring oscillator, asymmetric ring oscillator is used to obtain sub-ns timing resolution. Fig. 3 shows a simplified schematics and its timing diagram of the asymmetric ring oscillator. It only shows 8 stages but the actual chip implements 16 stages. The asymmetric ring oscillator was creates equally spaced even number (16) of timing signals.

The PLL circuit comprises a phase frequency detector (PFD), a charge pump, a loop filter (LPF), and a voltage-controlled oscillator (VCO; asymmetric ring oscillator in this case). An external capacitor ( $C_{vg}$ ) is required in the loop filter. The PLL has "divide by 2" counter, thus the frequency of the VCO is 80MHz. The propagation delay of the delay elements that determine the oscillation frequency of the VCO is controlled through a control voltage (VGN).

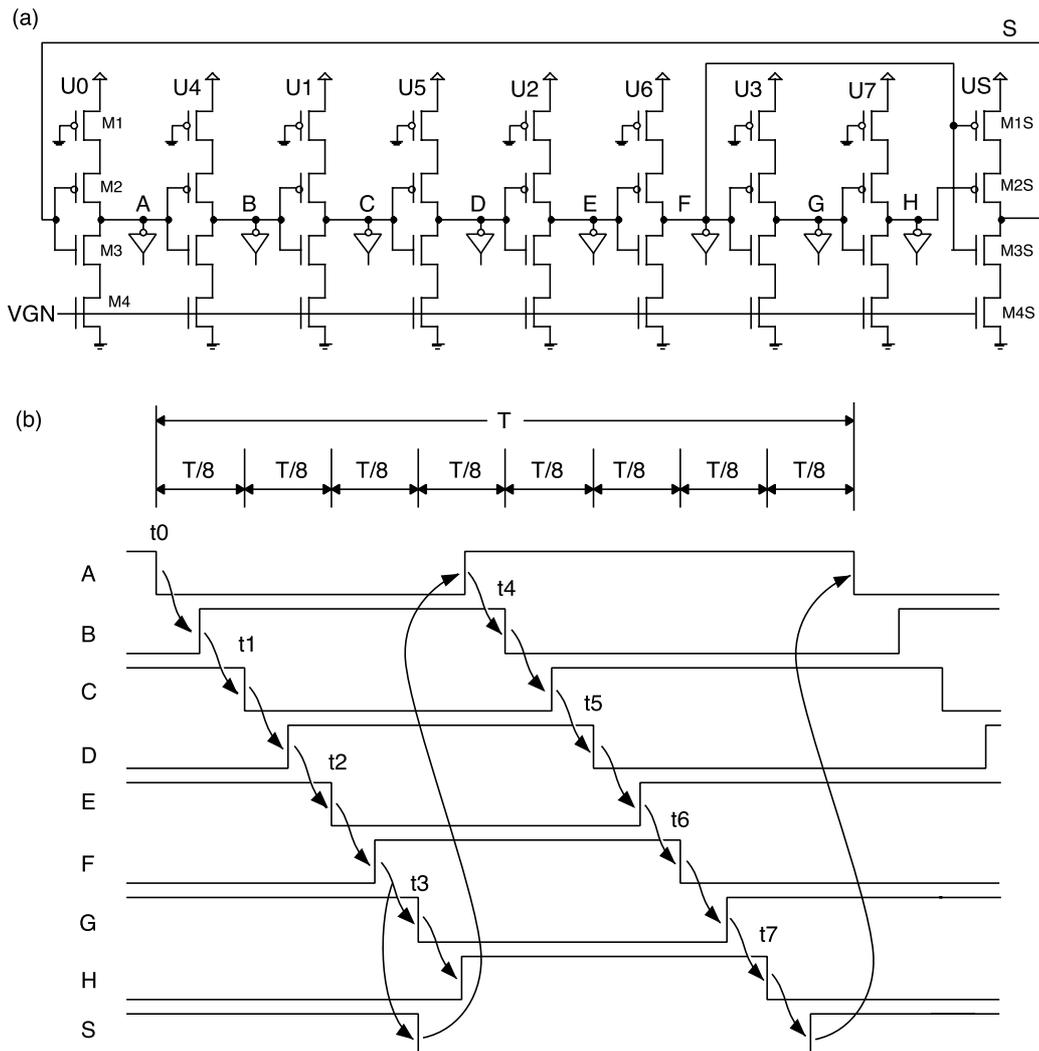


Fig. 3 (a) Asymmetric ring oscillator, (b) extracted timing signal.

## 4.2 Coarse Counter

The dynamic range of the fine time measurement is expanded by storing the state of a clock synchronous counter. The hit signal may though arrive asynchronously to the clocking and the coarse counter may be in the middle of changing its value when the hit arrives. To circumvent this problem two count values, 1/2 a clock cycle out of phase, are stored when the hit arrives (Fig. 4). Based on the fine time measurement from the PLL one of the two count values will be selected, such that a correct coarse count value is always obtained.

The coarse counter has 13 bits and is loaded with a programmable coarse time offset (the LSB is always 0) at reset. The coarse counter of the TDC is clocked by the two times higher frequency than the bunch crossing signal thereby the upper 12 bit of the coarse counter becoming a bunch count ID of the measurement.

The bunch structure of LHC is not compatible with the natural binary roll over of the 12 bit coarse time counter. The bunch counter can therefore be reset separately by the bunch count reset signal and the counter can be programmed to roll-over to zero at a programmed value. The programmed value of this roll-over is also used in the trigger matching to match triggers and hits across LHC machine cycles.

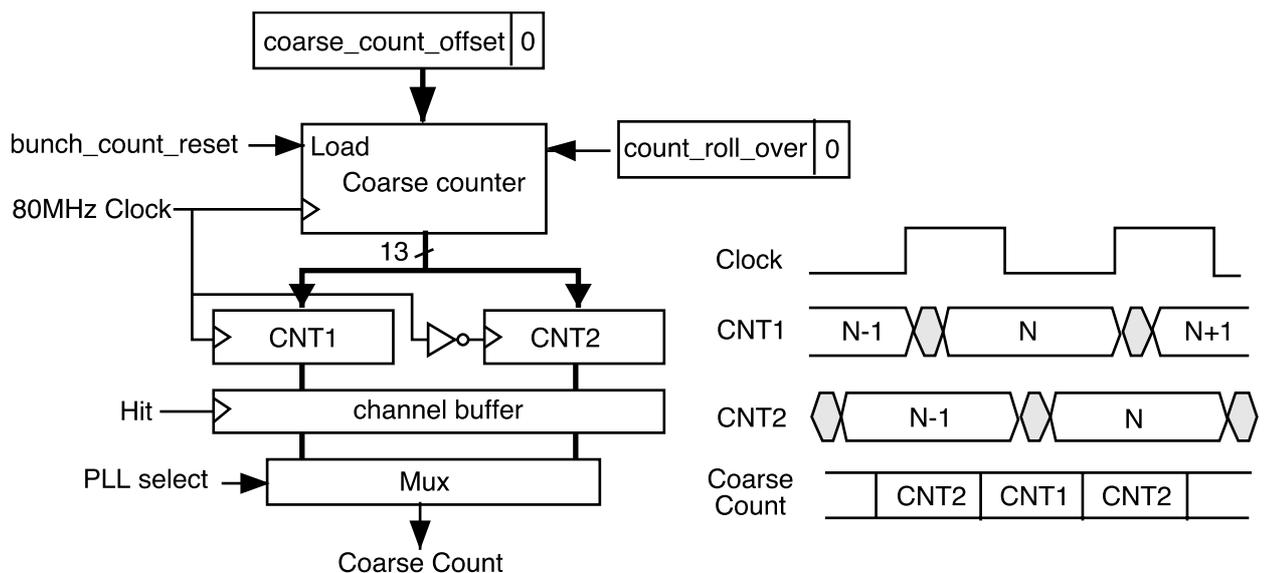


Fig. 4 Phase shifted coarse counters loaded at hit.

## 4.3 Channel Buffer.

Each channel can store 4 TDC measurements before being written into the common L1 buffer. The channel buffer is implemented as a FIFO controlled by an asynchronous channel controller. The channel controller can be programmed to digitize individual leading and/or trailing edges of the hit signal. Alternatively the channel controller can produce paired measurements consisting of one leading edge and the corresponding trailing edge.

If the channel buffer is full when a new hit arrives it will be ignored (rejected), but the information of the rejected hit is transferred with next valid hit. For the hits stored in the channel buffers to be written into the clock synchronous L1 buffer a synchronization of the status signals from the channel buffers is performed. Double synchronizers are used to prevent any metastable

state to propagate to the rest of the chip running synchronously at 40 MHz. When paired measurements of a leading and a trailing edge is performed the two measurements are taken off the channel buffer as one combined measurement.

#### 4.4 Encoder

When a hit has been detected on a channel the corresponding channel buffer is selected, the time measurement done with the ring oscillator is encoded into binary form (vernier time), the correct coarse count value is selected and the complete time measurement is written into the L1 buffer together with a channel identifier.

Although the ring oscillator and the coarse counter runs at 80 MHz, the base LHC clock is 40 MHz and bunch number is counted at 40 MHz. Most of logics in the AMT1 are designed to run at 40 MHz. To shift from 80 MHz to 40MHz regime, we would like to define different name to measured time. We call the upper 12 bit of the coarse counter as a ‘coarse time’, and the LSB of the coarse counter plus the vernier time as a ‘fine time’ as shown in Fig. 5. Thus the coarse time will be equivalent to the bunch count.

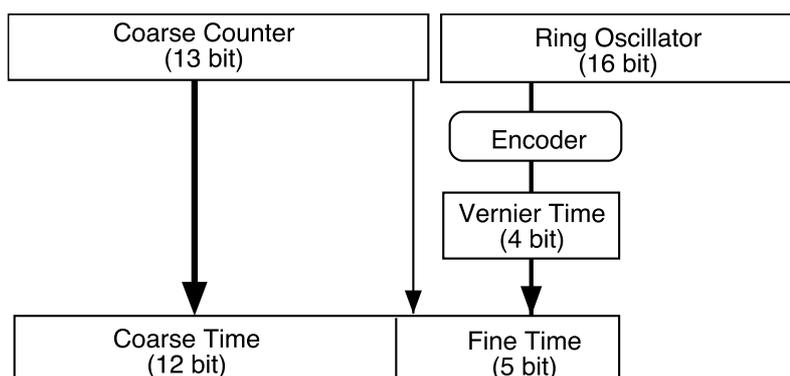


Fig. 5. Definition of coarse time and fine time.

In case a paired measurement of leading and trailing edge has been performed the complete time measurement of the leading edge plus a 8 bit pulse width is written into the L1 buffer. The 8 bit pulse width is extracted from the leading and trailing edge measurement taking into account the programmed roll-over value. The resolution of the width measurement is programmable.

When several hits are waiting in the channel buffers an arbitration between pending requests is performed. New hits are only allowed to enter into the active request queue when all pending requests in the queue have been serviced. Arbitration between channels in the active request queue is done with a simple hardwired priority (channel 0 highest priority, channel 23 lowest priority).

#### 4.5 L1 Buffer.

The L1 buffer is 256 hits deep and is written into like a circular buffer. Reading from the buffer is random access such that the trigger matching can search for data belonging to the received triggers. If the L1 buffer runs full the latest written hit will be marked with a special full flag. When the buffer recovers from being full the first arriving hit will be marked with a full

recover flag.

These flags are used by the following trigger matching to identify events which may have lost hits because of the buffer being full.

#### 4.6 Trigger Matching.

Trigger matching is performed as a time match between a trigger time tag and the time measurements themselves. The trigger time tag is taken from the trigger FIFO and the time measurements are taken from the L1 buffer. Hits matching the trigger are passed to the read-out FIFO.

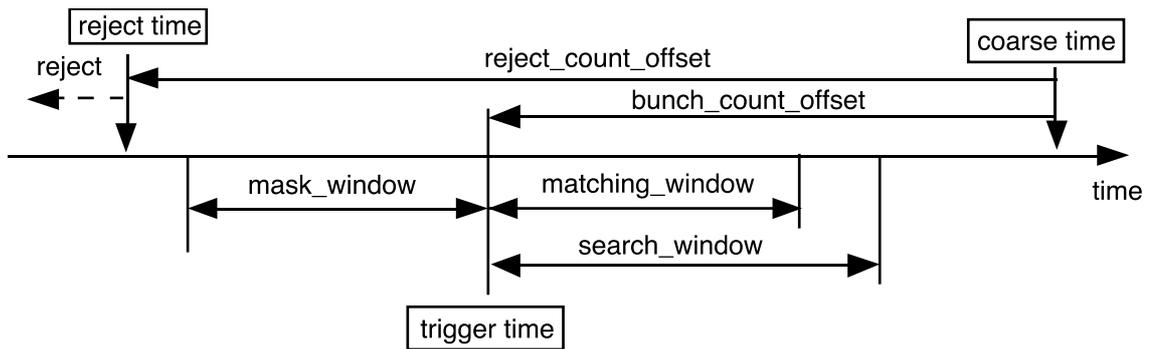


Fig. 6. Trigger latency and trigger window related to hits on channels. There are 3 time counters ; coarse time, trigger time and reject time counters.

A match between the trigger and a hit is detected within a programmable time window (Fig. 6). The trigger is defined as the coarse time count (bunch count ID) when the event of interest occurred. All hits from this trigger time until the trigger time plus the matching window will be considered as matching the trigger. The trigger matching being based on the coarse time means that the “resolution” of the trigger matching is one clock cycle (40MHz) and that the trigger matching window is also specified in steps of clock cycles.

The search for hits matching a trigger is performed within an extended search window to guarantee that all matching hits are found even when the hits have not been written into the L1 buffer in strict temporal order.

To prevent buffer overflow and to speed up the search time an automatic reject function can reject hits older than a specified limit when no triggers are waiting in the trigger FIFO. A separate reject counter runs with a programmable offset to detect hits to reject.

The trigger matching can optionally search a time window before the trigger for hits which may have masked hits in the match window. A channel having a hit within the specified mask window will set its mask flag. The mask flags for all channels are in the end of the trigger matching process written into the read-out FIFO if one or more mask flags have been set.

In case an error condition (L1 buffer overflow, Trigger FIFO overflow, memory parity error, etc.) has been detected during the trigger matching a special word with error flags is generated.

All data belonging to an event is written into the read-out FIFO with a header and a trailer. The header contains an event id and a bunch id. The event trailer contains the same event id plus

a word count.

#### 4.7 Trigger Interface.

The trigger interface takes care of receiving the trigger signal and generate the required trigger time tag to load into the trigger FIFO.

The basis for the trigger matching is a trigger time tag locating in time where hits belong to an event of interest. The trigger time tag is generated from a counter with a programmable offset. When a trigger is signaled the value of the bunch counter (trigger time tag) is loaded into the trigger FIFO (see Fig. 7).

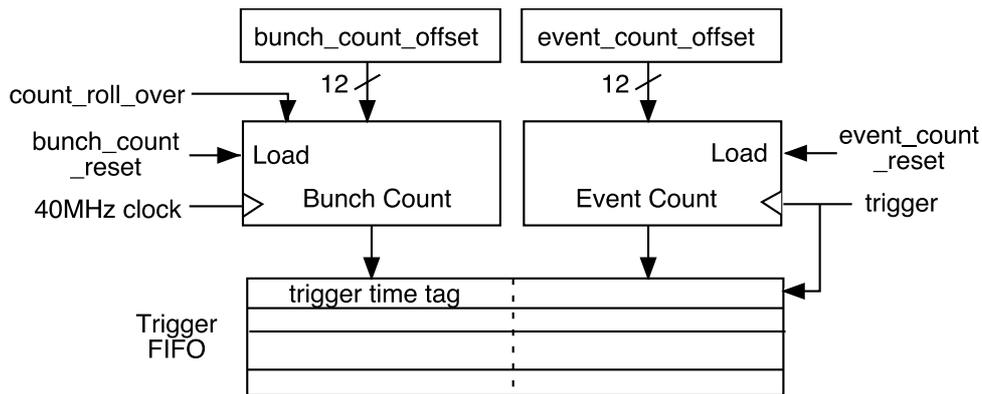


Fig. 7. Generation of trigger data.

If the trigger FIFO runs full the trigger time tags of following events will be lost. The trigger interface keeps track of how many triggers have been lost so the event synchronization in the trigger matching and the DAQ system is never lost. For each event with a lost trigger time tag the trigger matching will generate an event with correct event id and a special error flag signaling that the whole event has been lost.

#### 4.8 Encoded trigger and resets signal

Four basic signals are encoded using three clock periods (Table 1). The simple coding scheme is restricted to only distribute one command in each period of three clock periods. A command is signaled with a start bit followed by two bits determining the command. When using encoded trigger and resets an additional latency of three clock periods is introduced by the decoding compared to the use of the direct individual trigger and resets.

Table 1 Encoded signal bit pattern.

Meaning	bit		
	2	1	0
Trigger	1	0	0
Bunch count reset	1	1	0
Global reset	1	0	1
Event count reset	1	1	1

#### 4.9 Read-out FIFO.

The read-out FIFO is 64 words deep and its main function is to enable one event to be read

out while another is being processed in the trigger matching. If the read-out FIFO runs full there are several options of how this will be handled.

**Back propagate:**

The trigger matching process will be blocked until new space is available in the read-out FIFO. When this occurs, the L1 buffer and the trigger FIFO will be forced to buffer more data. If this situation is maintained for extended periods the L1 buffer or the trigger FIFO will finally become full and the measurement is stopped.

**Nearly full reject:**

In this mode the trigger matching will be blocked if either the L1 buffer or the trigger FIFO is nearly full. If this occurs event data will be rejected to prevent the L1 buffer and the trigger FIFO to overflow. The event header and event trailer data will never be rejected as this would mean the loss of event synchronization in the DAQ system. Any event which have lost data in this way will be marked with an error flag.

**Reject:**

As soon as the read-out FIFO full, event data (not event headers and trailers) will be rejected. Any loss of data will be signaled with an error flag.

#### 4.10 Serial Readout

All accepted data from the TDC can be read out via a serial read-out interface in words of 32 bits. The event data from a chip typically consists of a event header, accepted time measurements, mask flags, error flags (if any error detected for event being read out) and finally a event trailer.

The accepted TDC data can be transmitted serially over twisted pairs using LVDS signals. Data is transmitted in words of 32 bits with a start bit set to one and followed by a parity bit and a stop bit (Fig. 8). The serialization speed is programmable from 80 to 10 Mbits/s.

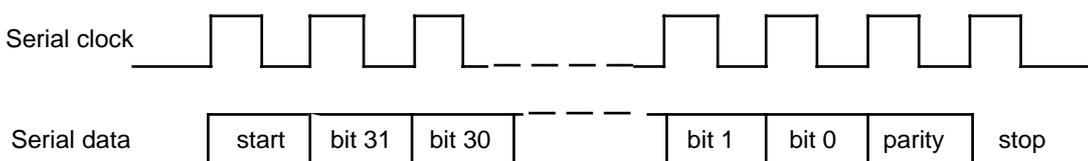


Fig. 8 Serial frame format with start bit and parity bit

In addition to the serialized data an LVDS pair can carry strobe information in a programmable format.

**Leading Strobe:** Direct serializing clock to strobe data on rising edge.

**DS Strobe :** DS strobe format as specified for transputer serial links. DS strobe only changes value when no change of serial data is observed.

#### 4.11 Packet format

Data read out of the TDC is contained in 32 bits data packets. The first four bits of a packet are used to define the type of data packet.

The following 4 bits are used to identify the ID of the TDC chip (programmable) generating the data. Only 7 out of the possible 16 packet types are defined for TDC data. The remaining 9 packet types are available for data packets added by higher levels of the DAQ system.

Some of the data format are shown below. Full description is available in the Users Manual [10]

**TDC header:** Event header from TDC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	TDC ID								Event ID								Bunch ID											

**TDC trailer:** Event trailer from TDC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	TDC ID								Event ID								Word Count											

**Mask flags:** Channel flags for channels having hits with in mask window

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	TDC ID								Mask flags																			

**Single measurement:** Single edge time measurement

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	TDC ID								Channel				T	E	Coarse Time								Fine Time					

T: Edge type. E: Hit error.

**Combined measurement:** Combined measurement of leading and trailing edge

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	TDC ID								Channel				Width				Coarse Time				Fine Time							

#### 4.12 Error monitoring.

All functional blocks in the TDC are continuously monitored for error conditions. Memories are continuously checked with parity on all data. All internal state machines have been implemented with a “one hot” encoding scheme and is checked continuously for any illegal state.

The JTAG instruction register have a parity check to detect if any of the bits have been corrupted during down load. The CSR control registers also have a parity check to detect if any of the bits have been corrupted by a Single Event Upset (SEU). The error status of the individual parts can be accessed via the CSR status registers.

Any detected error condition in the TDC sets its corresponding error status bit (Table. 2). All the available error flags are OR-ed together with individual programmable mask bits to generate an ERROR signal.

Table. 2. Description of Errors Flags

Error	bit#	Description
Coarse error	0	A parity error in the coarse count has been detected in a channel buffer.
Channel select error	1	A synchronization error has been detected in the priority logic used to select the channel being written into the L1 buffer.
L1 buffer error	2	Parity error detected in L1 buffer.
Trigger FIFO error	3	Parity error detected on trigger FIFO.
Matching state error	4	Illegal state detected in trigger matching logic.
Read-out FIFO error	5	Parity error detected in read-out FIFO.
Read-out state error	6	Illegal state detected in read-out logic.
Control parity error	7	Parity error detected in control registers.
JTAG error	8	Parity error in JTAG instruction.

### 4.13 JTAG Port.

JTAG (Joint Test Action Group, IEEE 1149.1 standard) boundary scan is supported to be capable of performing extensive testing of TDC modules while located in the system. Testing the functionality of the chip itself is also supported by the JTAG INTEST and BIST capability. In addition special JTAG registers have been included in the data path of the chip to be capable of performing effective testing of registers and embedded memory structures. Furthermore, it is also possible to access the CSR registers from the JTAG port.

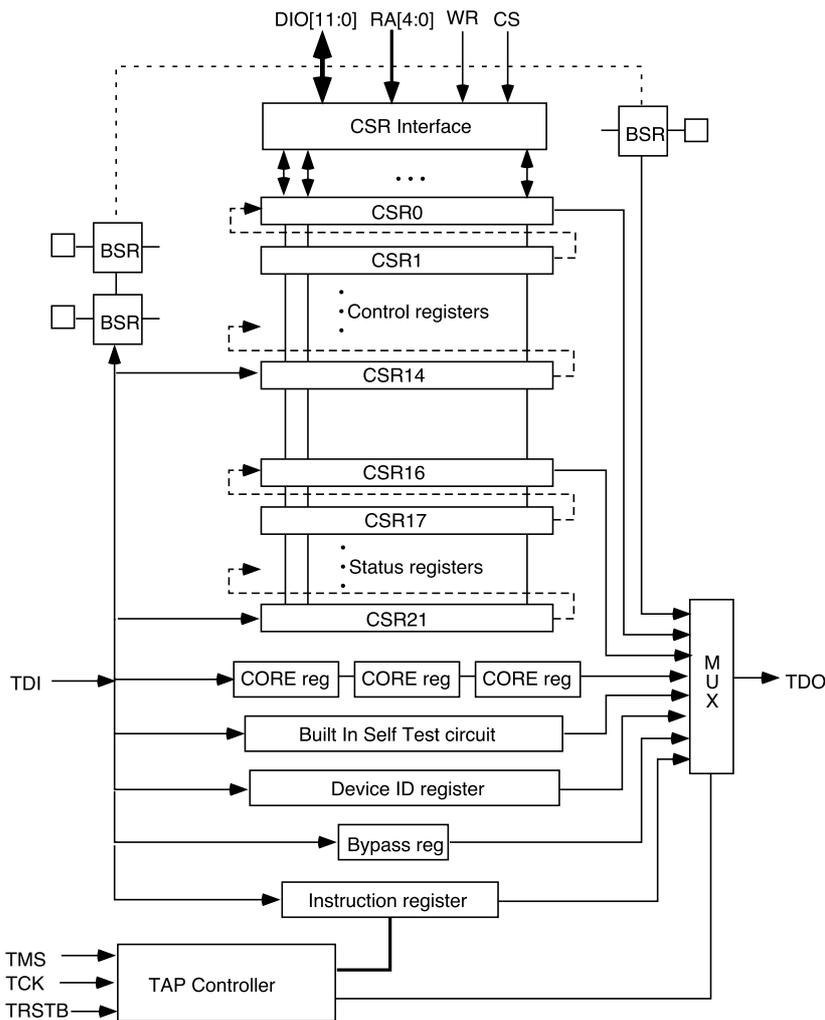


Fig. 9. Structure of JTAG - CSR registers.

#### 4.14 CSR Registers

There are two kinds of 12 bits registers, "CONTROL" and "STATUS" registers. The "CONTROL" registers are readable and writable registers which control the chip functionality. The "STATUS" registers are read only registers which shows chip statuses.

There are 15 Control registers (CSR0-14) and 6 Status registers (CSR16-21). These registers are accessible through 12bits bus and JTAG interface (Fig. 9). Bit assignments for the "CONTROL and "STATUS" registers are shown in Table. 3 and Table. 4 respectively.

Table. 3. Bit assignment of the control registers.

	BIT											
	11	10	9	8	7	6	5	4	3	2	1	0
CSR0	global_r eset	error_ reset	disable_ encode	enable_ errrst_ bcrevr	test_ mode	test_ invert	enable_ direct	disable_ ringosc	clkout_mode		pll_multi	
CSR1	mask_window											
CSR2	search_window											
CSR3	match_window											
CSR4	reject_count_offset											
CSR5	event_count_offset											
CSR6	bunch_count_offset											
CSR7	coarse_time_offset											
CSR8	count_roll_over											
CSR9	strobe_select		readout_speed		width_select			-	tdc_id			
CSR10	enable_ auto_ reject	enable_ lloccup _readout	enable_ match	enable_ mask	enable_ relative	enable_ serial	enable_ header	enable_ trailer	enable_ rejected	enable_ pair	enable_ trailing	enable_ leading
CSR11	enable_ rofull_ reject	enable_ llfull_ reject	enable_ trfull_ reject	enable_ ermark	enable_ mark_ rejected	enable_ ermark_ rejected	enable_ ermark_ _ovr	enable_ llovr_ _detect	enable_ mreset_ code	enable_ resetcb_ sepa	enable_ mreset_ evrst	enable_ setcount_ _bcrst
CSR12	enable_ sepa_ readout	enable_ sepa_ bcrst	enable_ sepa_ evrst	enable_ error								
CSR13	enable_channel[11:0]											
CSR14	enable_channel[23:12]											

Table. 4. Bit assignment of the status registers (read only).

	11	10	9	8	7	6	5	4	3	2	1	0
CSR16	rfifo_ empty	rfifo_ full	control_ parity	error_ flags								
CSR17	ll_ empty	ll_ nearly_ full	ll_ over_ recover	ll_ over flow	ll_ write_address							
CSR18	tfifo_ empty	tfifo_ nearly_ full	tfifo_ full	running	ll_ read_address							
CSR19	coarse_ counter [0]	tfifo_ occupancy		ll_ start_address								
CSR20	coarse_counter[12:1]											
CSR21	0	0	0	0	0	0	0	rfifo_ occupancy[5:0]				

## 5. Simulation Study

To get a feeling of the performance of a TDC in a real system it is required to perform simulations of the architecture using hits signals with realistic characteristics. Several simulations of the baseline TDC architecture under different conditions are done by using the Verilog simulator [2].

The baseline simulation conditions are the following:

- 20, 100, 300 kHz hit rate (2/3 random hits and 1/3 correlated hits)
- 100 kHz trigger rate
- drift time = 0 ~ 800 ns
- pulse width = 30 ~ 200 ns
- dead time = 600 ns
- trigger latency = 2.5  $\mu$ s
- mask & matching windows = 800 ns
- search window = 1200 ns
- reject offset = 4  $\mu$ s

### 5.1 Hit and trigger generation

Fig. 10 shows the distribution of number of hits matched with triggers with an average of 1.87 for the baseline conditions. This agrees well with the estimated value of :

$$\frac{\text{Matching Window (800 ns)}}{\text{Hit Interval}(10\mu\text{s})} \times \text{Tube Efficiency (96\%)} \times 24\text{ch} = 1.84 \text{ hits/trigger.}$$

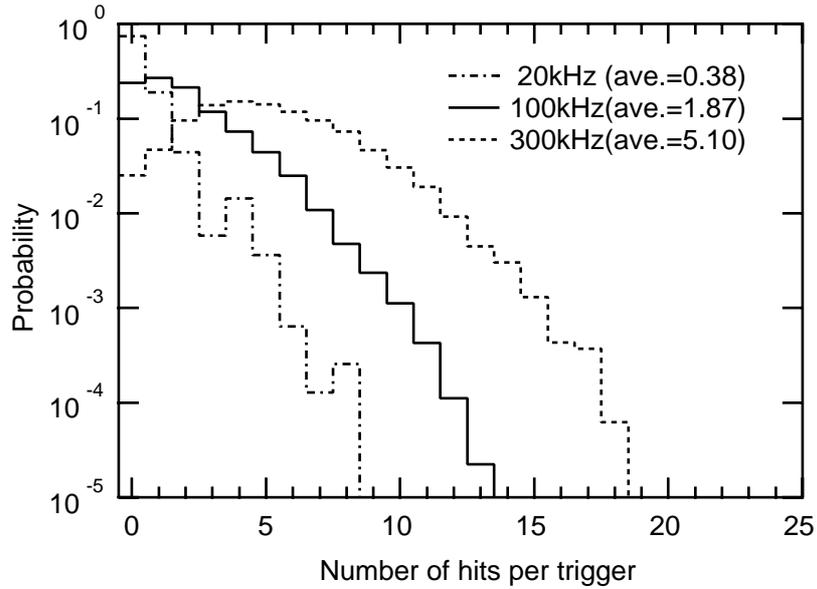


Fig. 10. Number of matched hits per trigger for 20, 100, and 300 kHz hit rate.

### 5.2 Channel buffer occupancy

Fig. 11 shows the occupancy of the channel buffer. For each arriving hit, the status of the hit registers are recorded. If the two hit registers are full at this moment, it means that the hit is rejected. The average occupancy is only  $2.1 \times 10^{-4}$  and  $8.3 \times 10^{-4}$  for 100 kHz and 300 kHz hit rates respectively. No missing hits have been seen in a one million hits simulation.

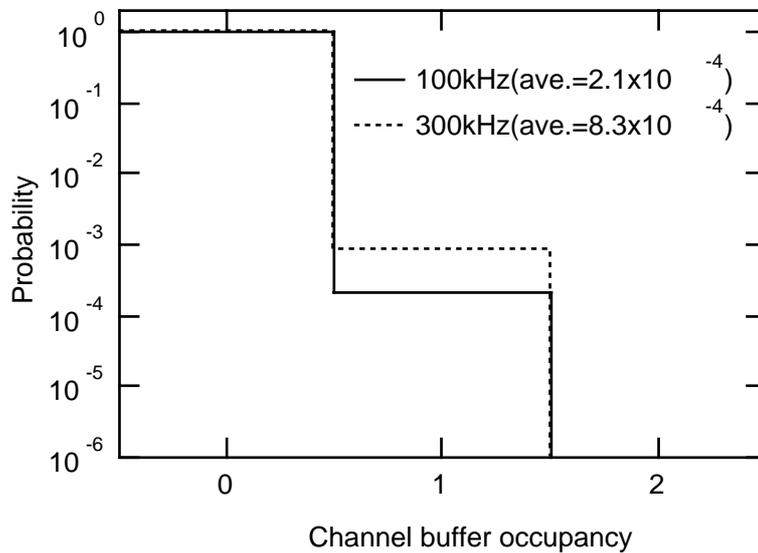


Fig. 11. Occupancy of channel buffer. Buffer occupancy 0 means there is no hits in the buffer when a new hit arrives; 1 means one waiting, and finally 2 means that a hit is rejected because the channel buffer is full.

### 5.3 First level buffer occupancy

The average level 1 buffer occupancy when not taking into account the processing needed for trigger matching can be found from:

$$24 \times \frac{\text{TriggerLatency } (2.5\mu\text{s}) + \text{Mask Window } (800 \text{ ns})}{\text{Hit Interval } (10\mu\text{s})} = 7.9 \text{ (@100KHz)}$$

The simulated first level buffer occupancy is shown in Fig. 12. Since the level 1 buffer length of the AMT is 256, there is almost no possibility to become full unless bandwidth of the data readout become tight.

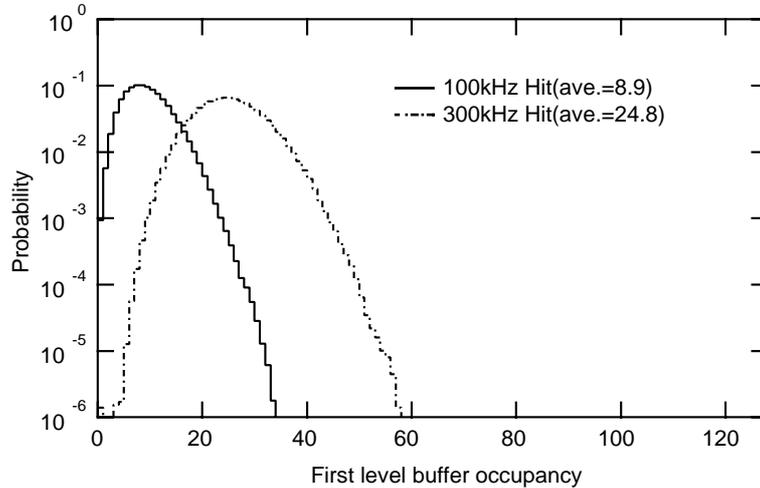


Fig. 12. Occupancy of the first level buffer. Level 1 buffer length of the AMT chip is 256.

#### 5.4 Trigger Search time

Fig. 13 shows the time needed to search for all hits corresponding to a trigger. In the baseline condition the average search time is 9.6 clock cycles and at 300 kHz hit rates 19.9 clock cycles (~500ns).

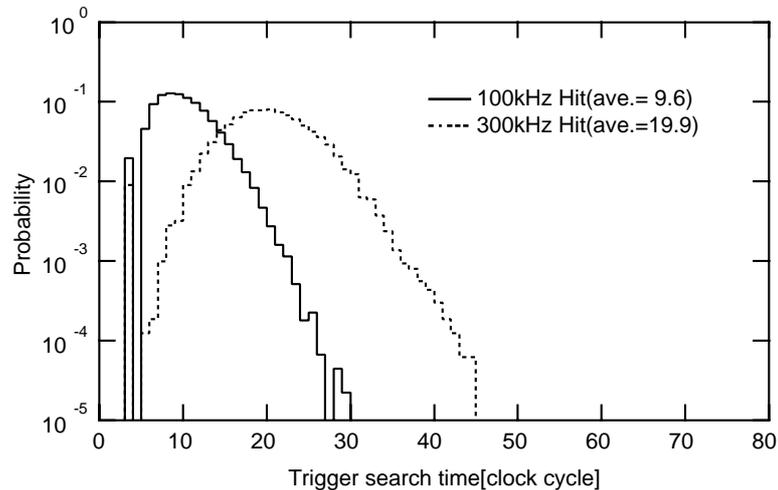


Fig. 13. Trigger search time for 100 kHz and 300 kHz hit rates.

#### 5.5 Trigger FIFO occupancy

Fig. 14 shows the occupancy of the trigger FIFO. Normally only one or two words are used, and there is little dependence on both the hit rate and the trigger rate. A trigger FIFO depth of 8 seems more than sufficient under these conditions.

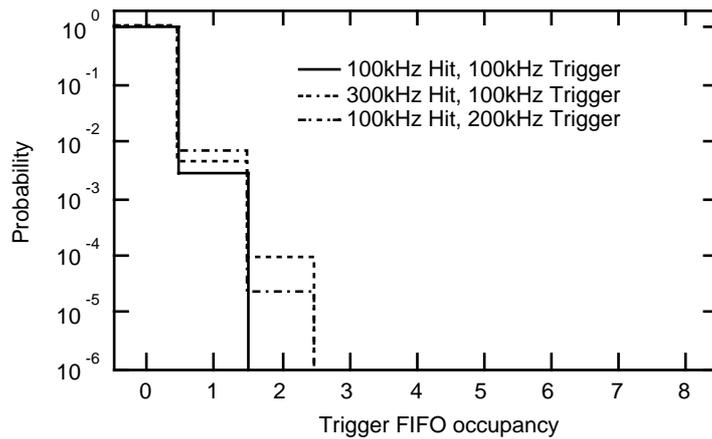


Fig. 14. Trigger FIFO occupancy for various conditions.

## 5.6 Readout Buffer occupancy

...

## 6. Prototype Performance

To measure the basic performance of the design and confirm the radiation tolerance of the process, we have developed a test element group chip (AMT-TEG) using the 0.3  $\mu\text{m}$  process at first. After the successful test of the AMT-TEG, we proceeded to develop full-functional AMT chip (AMT-1).

AMT-TEG contains bare NMOS and PMOS transistors, a ring oscillator for radiation tests. Gamma-ray irradiation was performed with a  $\text{Co}^{60}$  source at Tokyo Metropolitan University. Neutron irradiation was performed at the PROSPERO reactor in France.

Photograph of the AMT-1 is shown in Fig. 15.

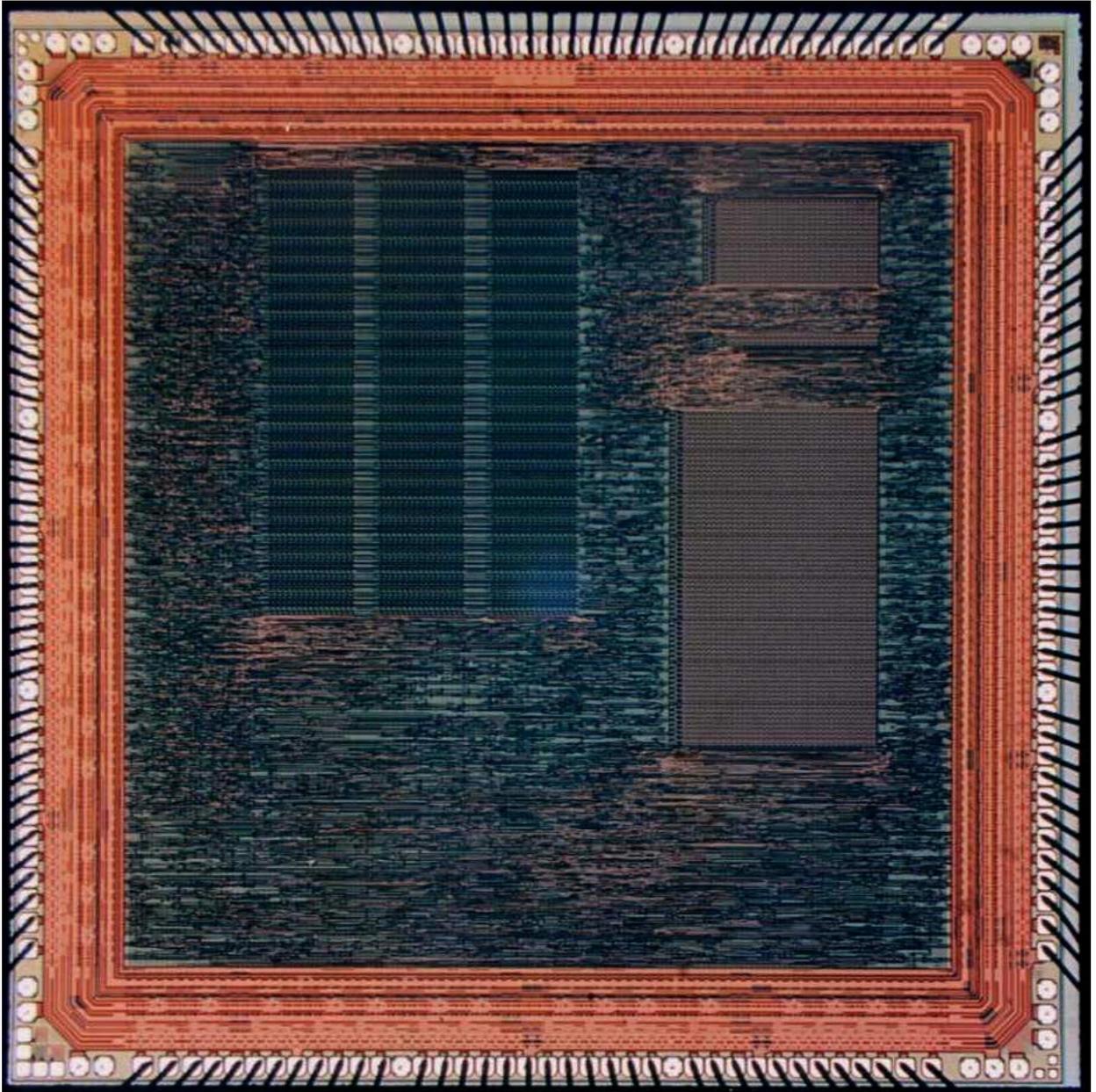


Fig. 15 Photograph of the AMT-1 chip. Die size is about 6mm by 6mm.

### 6.1 PLL and Ring Oscillator

Although the chip is designed in a gate-array technology, layout of the time critical parts such as PLL and the asymmetric ring oscillator were designed manually to achieve high resolution. We determined the jitter of the PLL circuit by measuring the oscillation period of each cycle. RMS values of the measurements versus frequency and power supply voltage are plotted in Fig. 16 (a) and (b) respectively. The jitter of the PLL is small ( $< 140$  ps) and stable for the 40-120 MHz frequency range and for supply voltages between 2.8 - 3.8 V (normal operating condition is 80 MHz and 3.3V respectively).

The jitter shows a small structure around 90 MHz and the value is a little worse than that of the previous chip [12] which was fabricated in a  $0.5 \mu\text{m}$  process. However the jitter is still small enough for the MDT detector which requires 500 ps resolution. Additional attention will be directed to the layout around the PLL in next chip to achieve better stability.

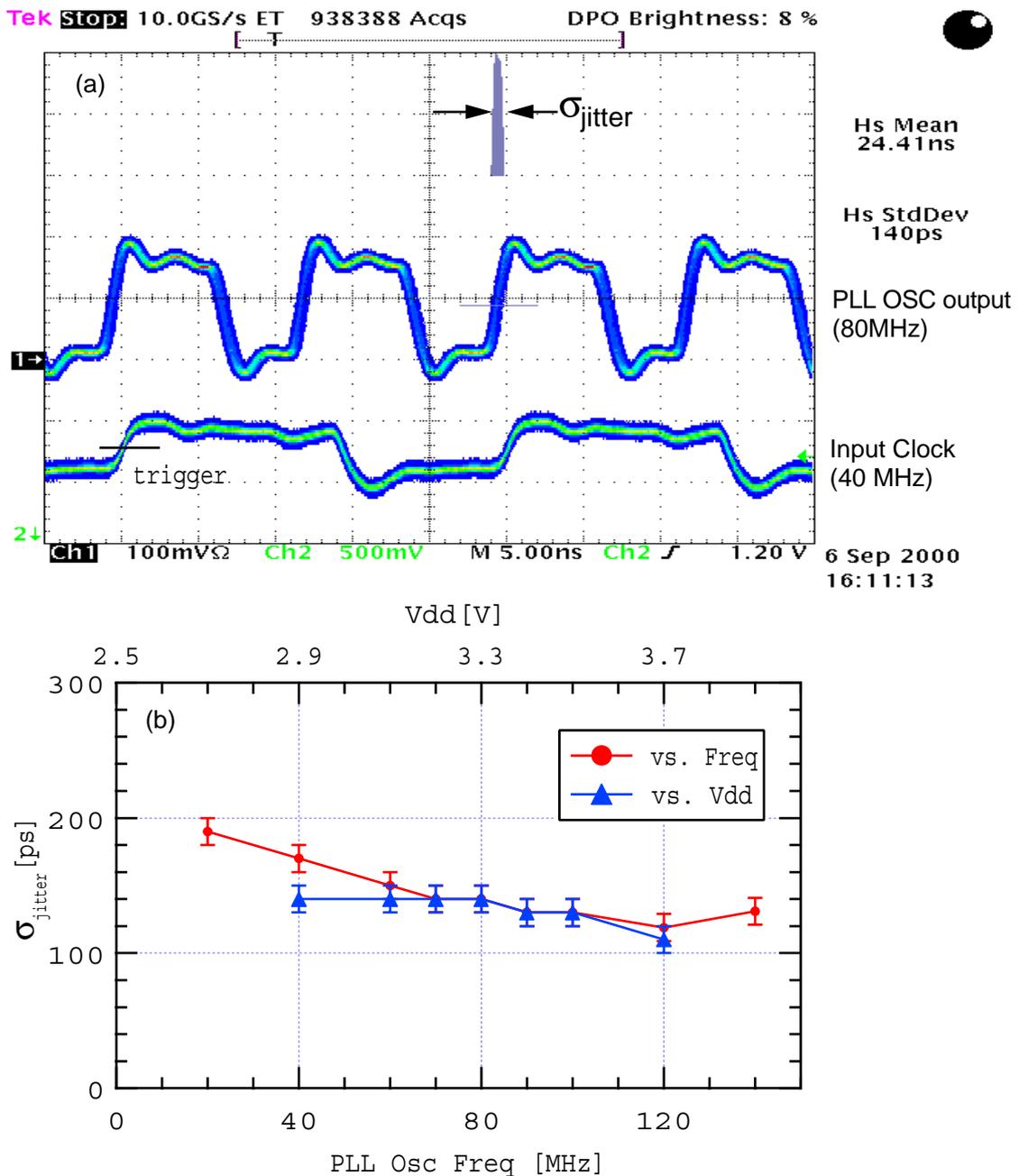


Fig. 16 Waveform of the input clock and PLL oscillation. PLL jitter is measured relative to the input clock. (b) Stability of the PLL vs. oscillation frequency and supply voltage.

## 6.2 Channel Buffer

Recording speed of the channel buffer is important to have a good double pulse resolution or edge separation. Minimum edge separation was determined by reducing pulse width and pulse separation until the hit information is lost.

Fig. 17 shows an example of minimum pulses. Two leading and two trailing edge timing are successfully recorded in the 4 word channel buffer. Since the test instruments can not generate pulses shorter than 5 ns, actual performance of the chip may be better than 5 ns, which is already far better than the MDT requirement.

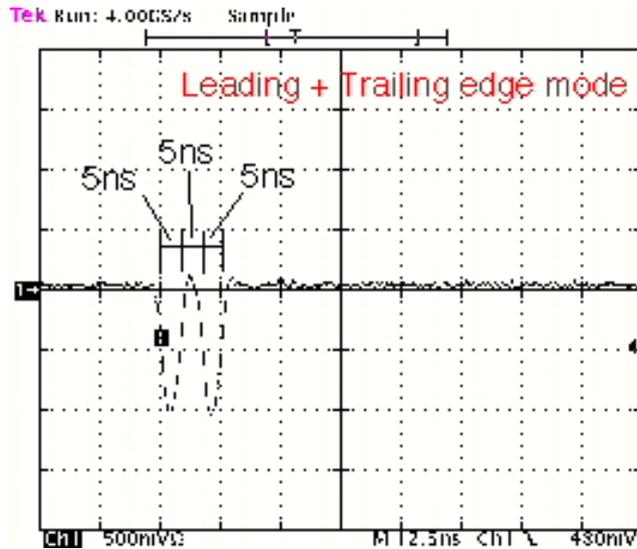


Fig. 17 Minimum pulses successfully recorded in the AMT chip.

The data transfer speed from the channel buffer to the first level buffer is an essential part of this TDC architecture. If the channel buffer become full, further hit information will be lost. In a Verilog simulation, the probability of hit loss is very low ( $< 10^{-6}$ ) for 300 kHz input rate in all channels. The transfer speed is measured by changing the number of simultaneous hit channels and determining the minimum hit interval where all hits are accepted.

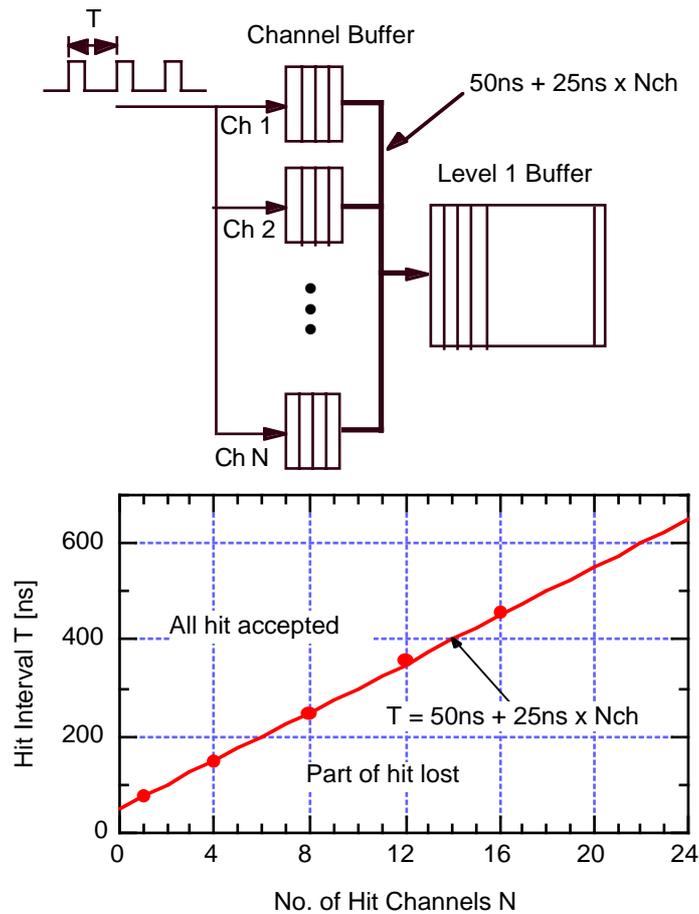


Fig. 18 Minimum hit interval for simultaneous hit inputs. System clock cycle is 25 ns. The data points show minimum hit intervals and the straight line indicates the expected performance from the 2 cycles plus N cycles required by the design.

In Fig. 18 minimum hit interval for N channel simultaneous inputs are plotted. Above the data point all hit information is recorded, but if the hit interval is reduced less than the data point, a part of the hit information become lost due to the lack of the transfer capability. The line in the figure shows expected speed from the circuit. We see the overhead for arbitration is only 2 cycle and successive data transfer occurs at each cycle.

### 6.3 Time Resolution and Non-Linearity

Time resolution was measured by supplying a clock synchronous hit signal to the input and varying the delay time of the signal. The result is shown in Fig. 19. The RMS value of 305 ps is obtained.

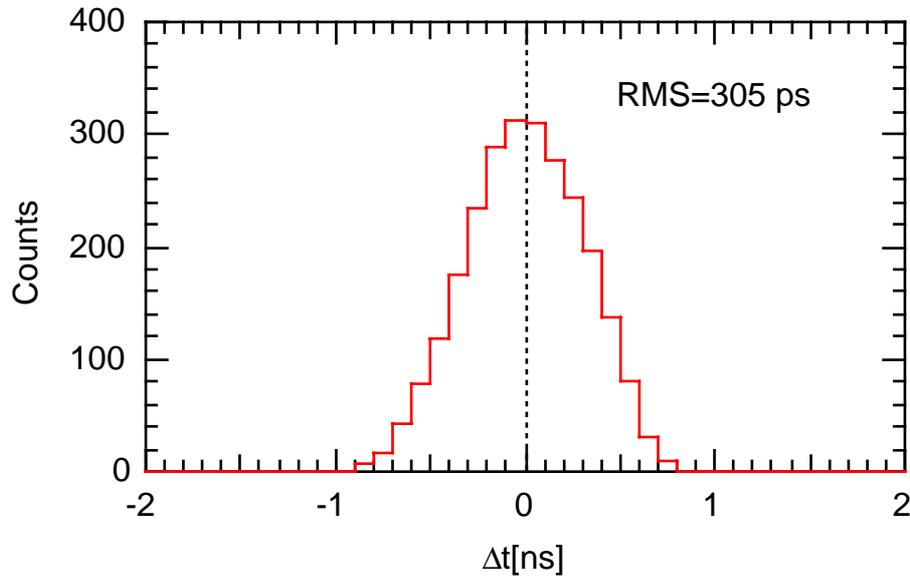


Fig. 19 Time resolution measurement. Input clock frequency is 40 MHz and time bin is 781.25 ps/bit. The data contains digitization error of 225 ps.

Non-linearity of the time measurement was measured by applying a hit signal for which the delay time is uniformly distributed, and counting the number of hits recorded in each bin. The Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are shown in Fig. 20 (a) and (b) respectively. Both are small enough (RMS < 70 ps) for our purpose.

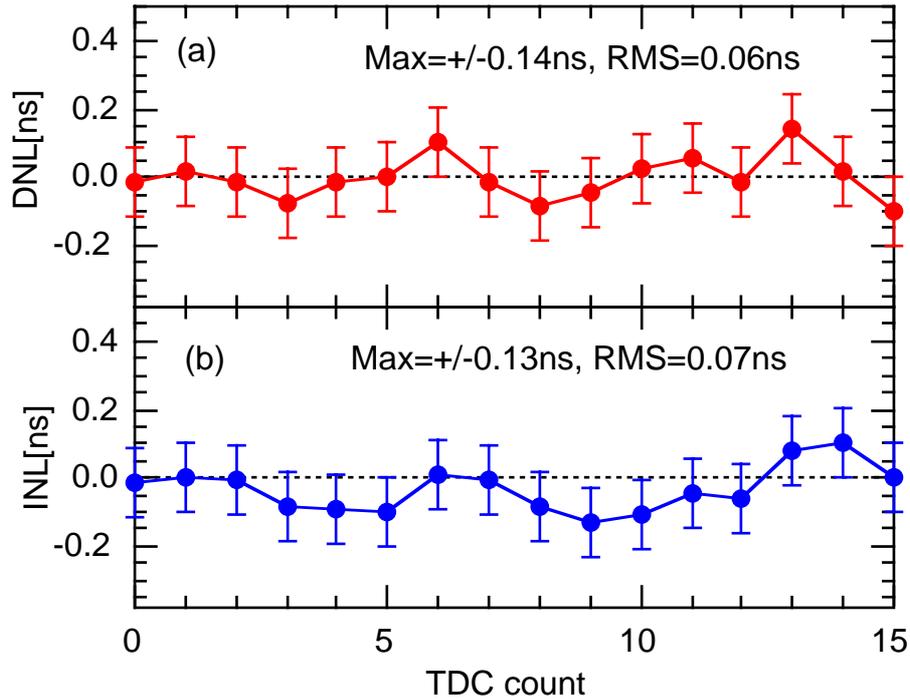


Fig. 20 (a) Differential non-linearity, and (b) Integral non-linearity measurement.

## 6.4 Power Consumption

Power consumption of the AMT-1 chip was measured at 400 kHz hit rate for 24 channels and 100 kHz trigger rate. The results is;

$$3.3\text{V} \times 148 \text{ mA} = 488 \text{ mW/chip} (\sim 20\text{mW/chan})$$

This value is a factor of two larger than the target value. Main source of the power consumption is LVDS receiver. Since the LVDS receiver was newly developed at Toshiba, we only noticed at last stage that it consumes much power than we expected. Estimated power consumption of the LVDS receiver with HSPICE is 15 mW/LVDS receiver.

A new LVDS receiver is now under development which consumes only 1/4 of the present receiver.

## 6.5 TDC IRRADIATION TEST

### Gamma-ray Irradiation

Gamma-ray irradiation test was done at Tokyo Metropolitan University with a  $\text{Co}^{60}$  source. The irradiation rate was about 90 rad(Si)/sec, and total dose irradiated was 100 krad(Si). During the irradiation so called worst bias conditions for MOS transistors ( 3.3 V is applied to NMOS gate, and no voltage is applied to PMOS gate), were used. To study post-radiation effects, parametric measurements were also done after annealing (1 week at 100 degree C) following the MIL-STD-883 method [13].

Total dose expected for worst location of the MDT electronics is 11 krad(Si) for 10 years

LHC operation (including a factor 4 safety factor) [9].

In a sub-micron process, most severe damage from the ionization process is an increase of leakage current. Fig. 21 shows drain leak current for NMOS and PMOS transistors. An increase of NMOS drain leak current above 25 krad(Si) was seen while no increase is seen in PMOS. Recovery of the pre-radiation condition is seen after the annealing in NMOS.

Threshold voltage shifts of transistors are shown in Fig. 22. There is no shift seen in PMOS transistors and a NMOS transistor while small shifts (~100 mV) are seen in two NMOS transistors. Since these transistors do not have any protection circuit, the transistors are susceptible to damage. More samples are needed to confirm whether the shift is due to the irradiation or not.

Fig. 23 shows variation of oscillating frequency of a ring oscillator and supply current. The ring oscillator is composed of 33 NAND gates. The oscillating frequency becomes lower above 50 krad(Si). The total chip current was also increased above 50 krad(Si).

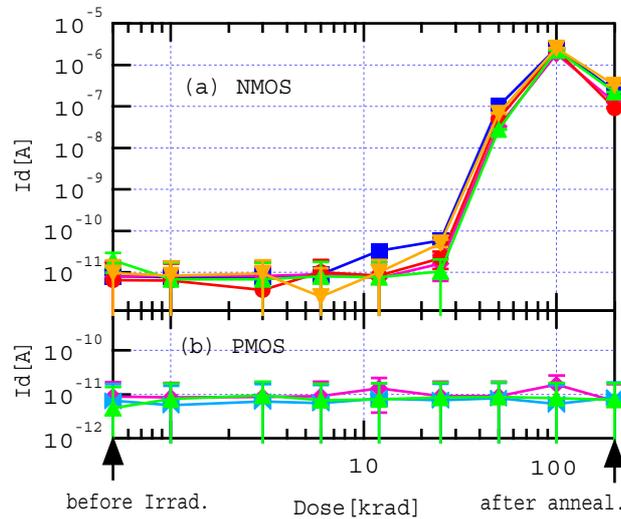


Fig. 21 Drain leakage current of (a)NMOS and (b)PMOS transistors. Left-most and right-most points show the value before irradiation and after 1 week at 100°C annealing respectively

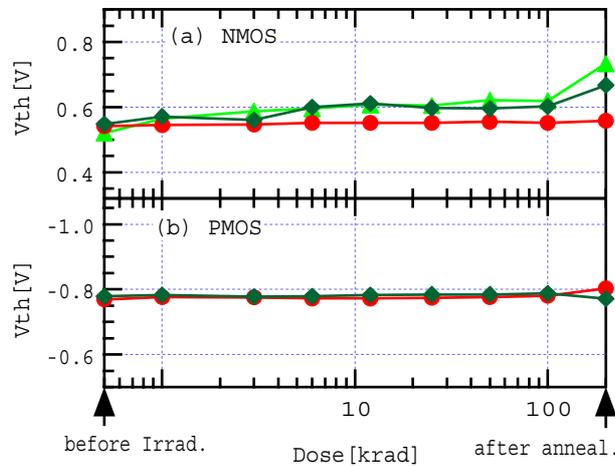


Fig. 22 Threshold voltage shifts of (a)NMOS and (b)PMOS transistors.

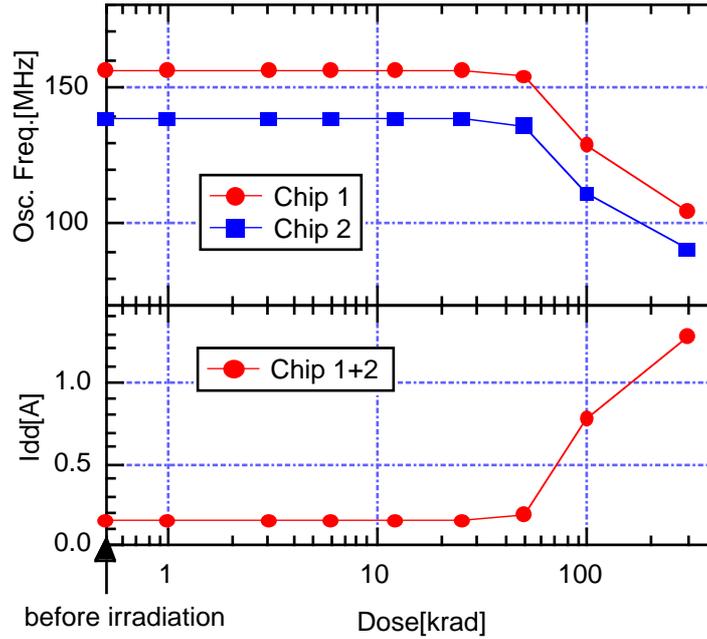


Fig. 23 (a) Oscillation frequency of a ring oscillator, (b) Total current of two chips. Left-most points show the value before irradiation.

### Neutron Irradiation

Neutron irradiation was done at the PROSPERO reactor facility in France. Eight chips were exposed to neutron flux of  $1.0 \times 10^{13}$  and 4 chips were exposed to  $1.6 \times 10^{13}$  n/cm<sup>2</sup> (1 MeV neutron equivalent). During the neutron exposure, chips are placed in a conductive plastic case. The expected neutron flux at MDT front-end electronics for 10 years of LHC operation is less than  $1.2 \times 10^{13}$  n/cm<sup>2</sup>.

After cooling of the radioactivity ( $\sim 2$  months), we measured transistor parameters and ring oscillator frequency. We have not observed any apparent change in all sample chips.

### hadrons (Single Event Upset)

We have not yet measured Single Event Effect (SEE) cross section for the AMT. The estimated fluence for hadrons of energy greater than 20 MeV is about  $10^{10}$  /cm<sup>2</sup>/10years [9].

If we assume a SEU (Single Event Upset) cross section of  $10^{-13}$ /cm<sup>2</sup>/bit, we will have 1.5 SEU/day/MDT for the contents of CSR. This value is not so large. As for the data we will have 0.2 SEU/day/MDT for Data. This value is smaller than that of the CSR since valid data reside within the chip for very short time.

Furthermore, in the AMT, 1 bit SEU is detectable by parity checking. Anyway we need to measure cross section for the SEE.

## **7. Remaining Developments**

Although the AMT-1 chip shows excellent performance and fulfils most of requirements, there are several items to be improved and to be added.

### 7.1 Low Power LVDS receiver

Power consumption of present LVDS receiver is rather large (~15 mW), and this should be reduced. A new LVDS receiver has been developed, and DC current and propagation delay are shown in Fig. 24 and Fig. 25 respectively.

DC currents for old and new LVDS receivers at Vicm (input center voltage) = 1.2 V are 4.8 mA (16 mW) and 1.2 mA (4mW) respectively. Thus the power consumption is reduced a quarter of previous design. Furthermore the propagation delay is also reduced a factor of 3.

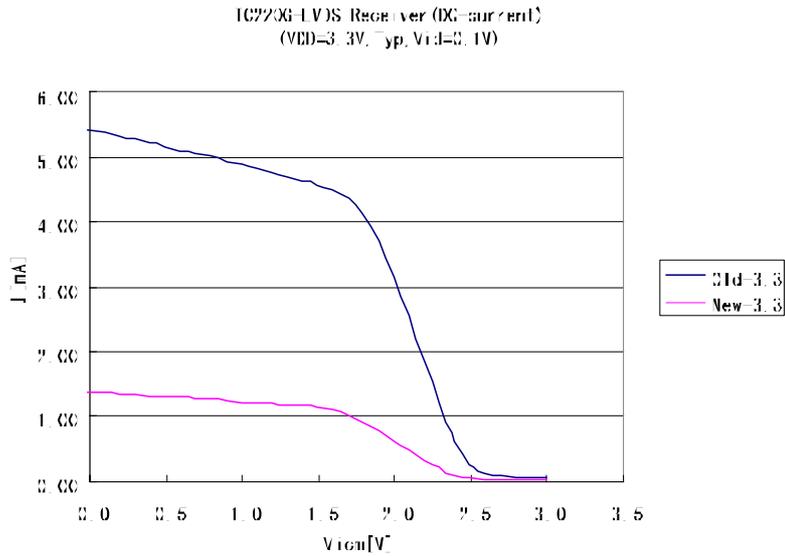


Fig. 24 DC current comparison between old and new LVDS receiver.

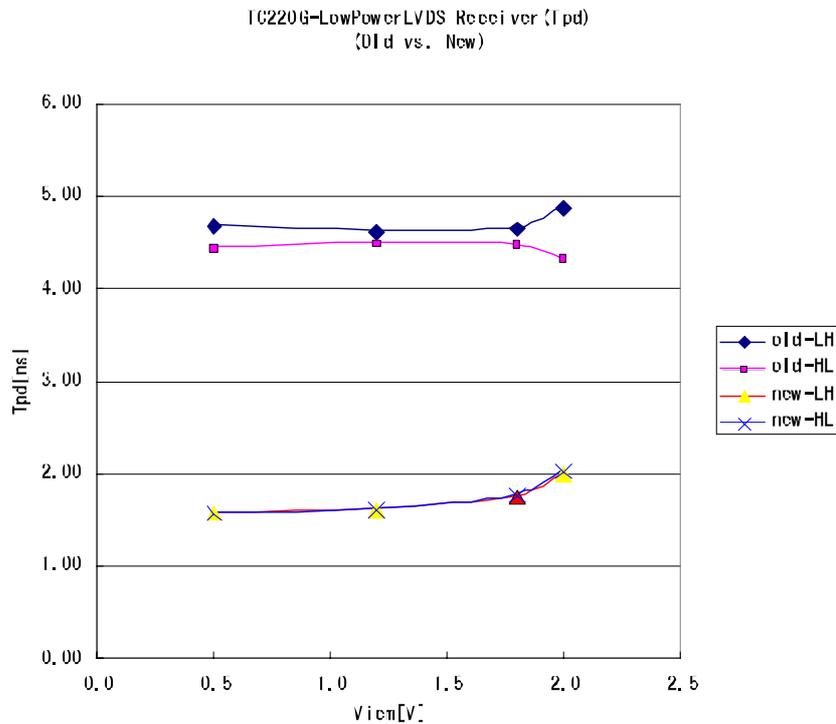


Fig. 25 Propagation delay comparison between old and new LVDS receiver.

## 7.2 JTAG control circuit for the ASD

Design of the ASD requires an external JTAG to serial controller [14] to access internal registers of the ASD. Original plan is to use a FPGA device in the mezzanine board (Fig. 26-(a)). Since the AMT already have JTAG controller, we decided to include the interface in the AMT chip (Fig. 26-(b)).

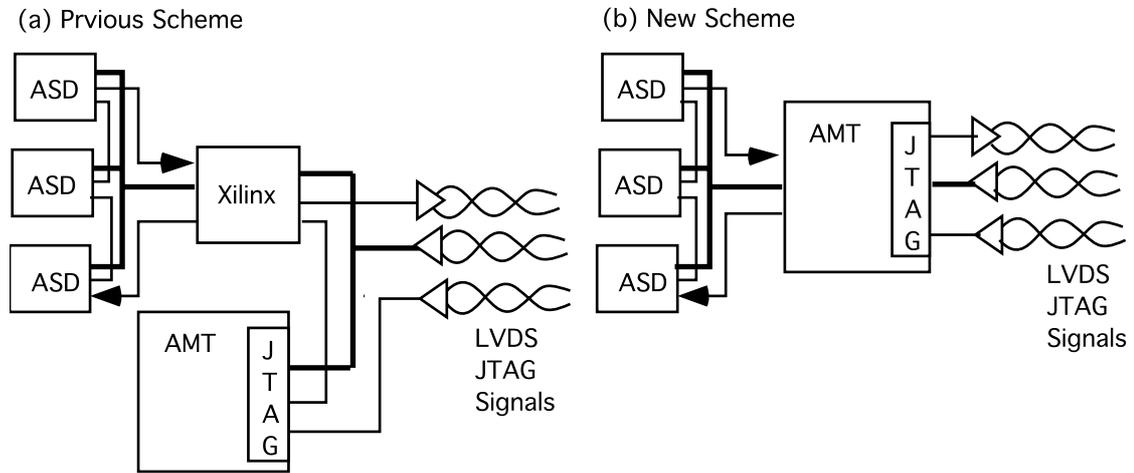


Fig. 26 (a) Previous JTAG connection scheme and (b) new scheme.

## 8. Schedule

AMT development and production schedule is shown in Fig. 27.

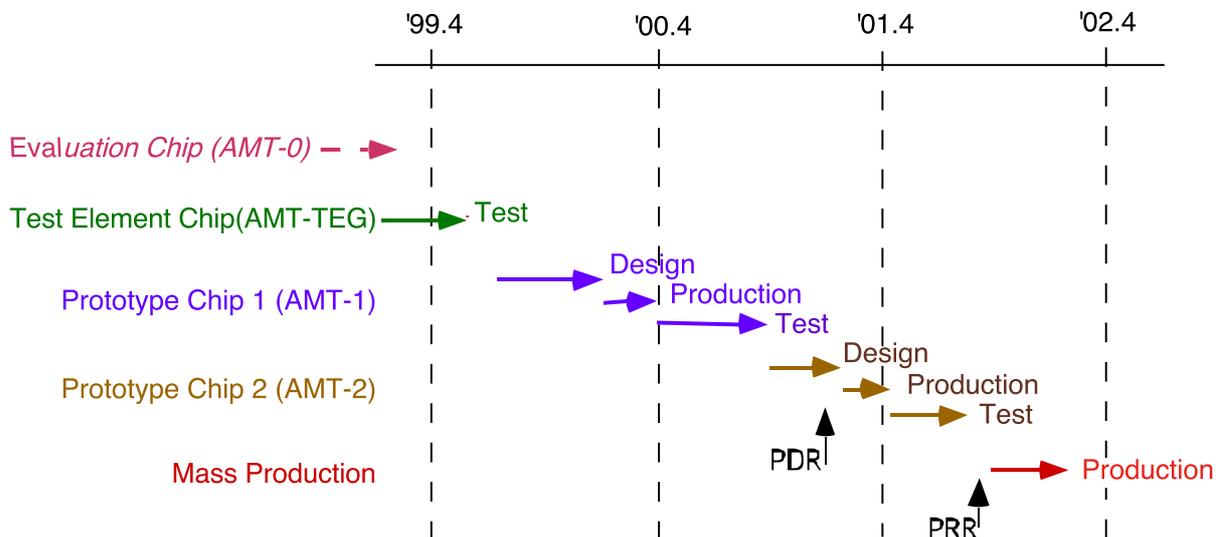


Fig. 27 Schedule of the AMT development and production.

## 9. References

- [1] Y.Arai and J. Christiansen, "Requirements and Specifications of the TDC for the ATLAS Precision Muon Tracker", ATLAS Internal Note, MUON-NO-179, 14 May 1997.
- [2] Y.Arai and J. Christiansen, "TDC Architecture Study for the ATLAS Muon Tracker", Proceedings of the Third Workshop on Electronics for LHC Experiments, London, Sep. 1997. CERN/LHC/97-60, pp315-319.

- 
- [3] J. Christiansen, "AMT-0 User Manual", <http://atlas.kek.jp/~arai/amt0/>.
- [4] Y. Arai, "Performance and Irradiation Tests of the 0.3 mm CMOS TDC for the ATLAS MDT", Proceedings of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, 1999. CERN/LHCC/99-33, pp 462-466.
- [5] Y. Arai, "Development of Frontend Electronics and TDC LSI for the ATLAS MDT", 7th International Conference on Instrumentation for Colliding Beam Physics Hamamatsu, November 15-19, 1999, Nucl. Instr. Meth. A. Vol. 453, pp. 365-371 (2000).
- [6] John Huth, John Oliver, Werner Riegler, Eric Hazen, Christoph Posch, Jim Shank, "Development of an Octal CMOS ASD for the ATLAS Muon Detector", Proceedings of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, 1999. CERN/LHCC/99-33, pp. 436-442.
- [7] J., Chapman and Bob Ball, "Options for MDT connections", Nov. 1998 Draft.
- [8] Trigger and DAQ Interfaces with Front-End Systems: Requirement Document, Version 1.0, Atlas Trigger-DAQ Steering Group, January, 1996.
- [9] Atlas policy on radiation tolerant electronics, ATLAS Radiation Tolerance Criteria (Rev 2). <http://www.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm>
- [10] AMT-1 User's Manual, <http://atlas.kek.jp/~arai/ATLAS/>
- [11] AMT-1 Data Sheets, <http://atlas.kek.jp/~arai/ATLAS/>
- [12] Y. Arai and M. Ikeno, "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", IEEE Journal of Solid-State Circuits, Vol. 31, No. 2, Feb. 1996, p.212-220.
- [13] Test Method and Procedures for Microelectronics, MIL-STD-883, Method 1019.4.
- [14] Christoph Posch, "MDT-ASD: Serial data I/O and programmable parameters", [http://bmc.bu.edu/bmc/asd/octal/spec/ASD00A\\_Prog.PDF](http://bmc.bu.edu/bmc/asd/octal/spec/ASD00A_Prog.PDF).