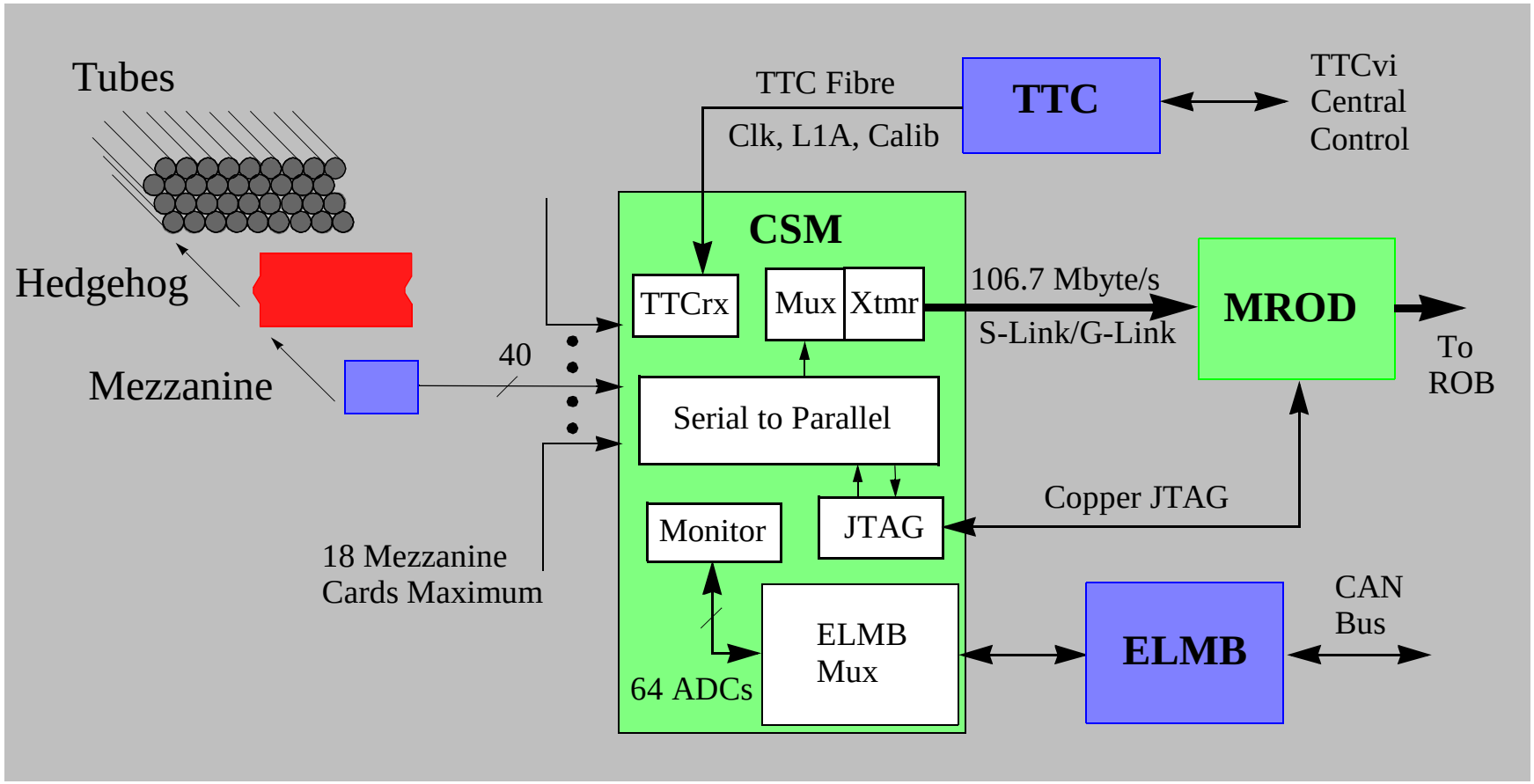
A CSM centered view of the Front-End

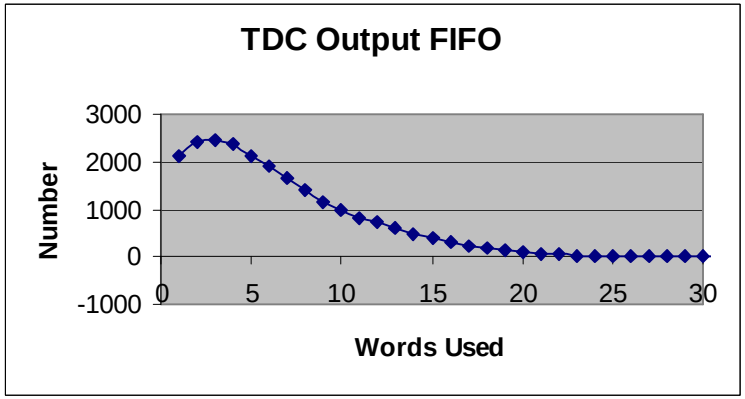
J. Chapman - February 2001

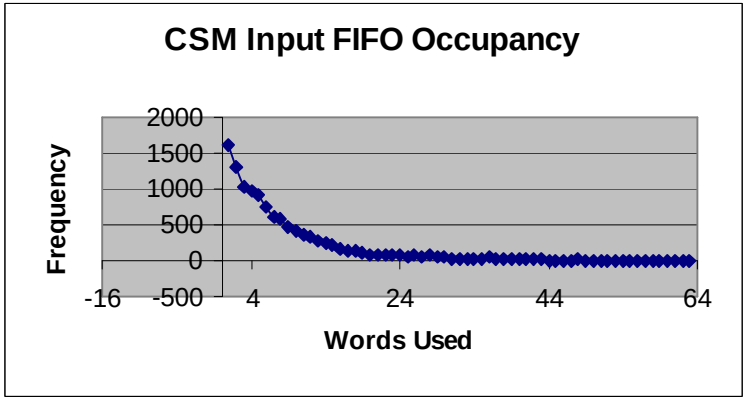
- CSM Interactions with ASD/TDC/TTC/DCS/MROD

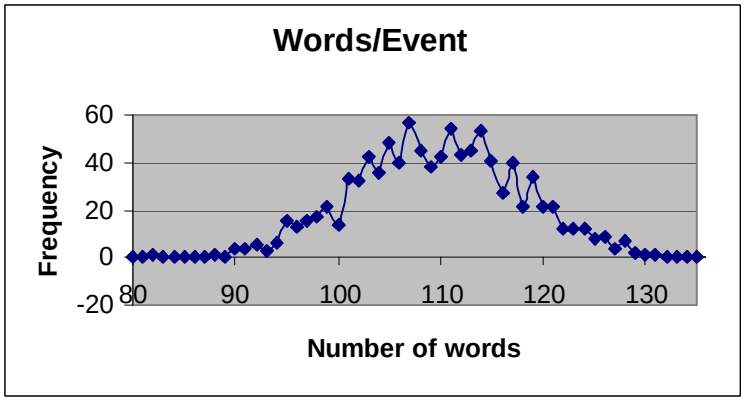


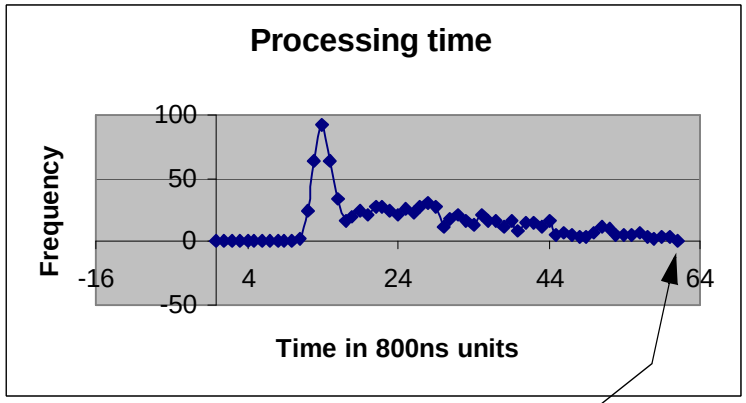
Began with VerilogHDL Simulations

Data from 75kHz trigger with 5 hits/TDC*









Note the maximum time is ~50ms

* Simulation done with non-pipelined design - current pipelined design moves data more than twice as fast, limited by TDC output.

CSM Design Choices

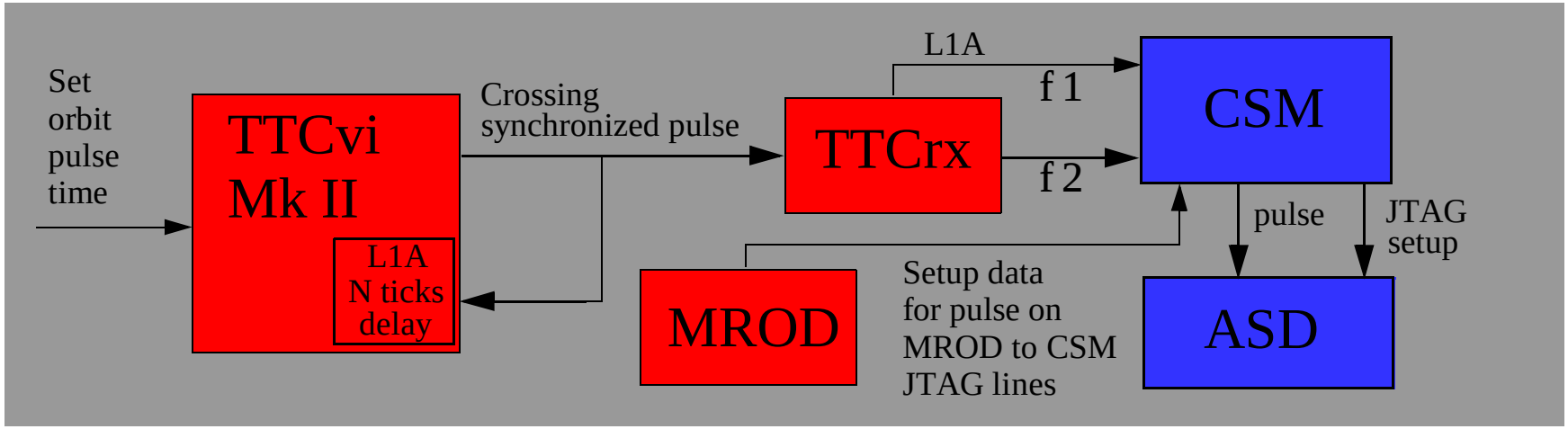
- Initialization - Cat5 Cable JTAG from MROD (Opto-isolate)
- Environment Monitoring - ELMB Analog Mux (64 channels)
- Calibration - Standard TTC System (vernier using 2nd phase)
- Link to ROD - Low Power G-Link at 53.3MHz
- Simple time division multiplexing
- 1.8 volt LVDS capable FPGA
- Clock phase alignment with built in DLLs

Initialization Requirements

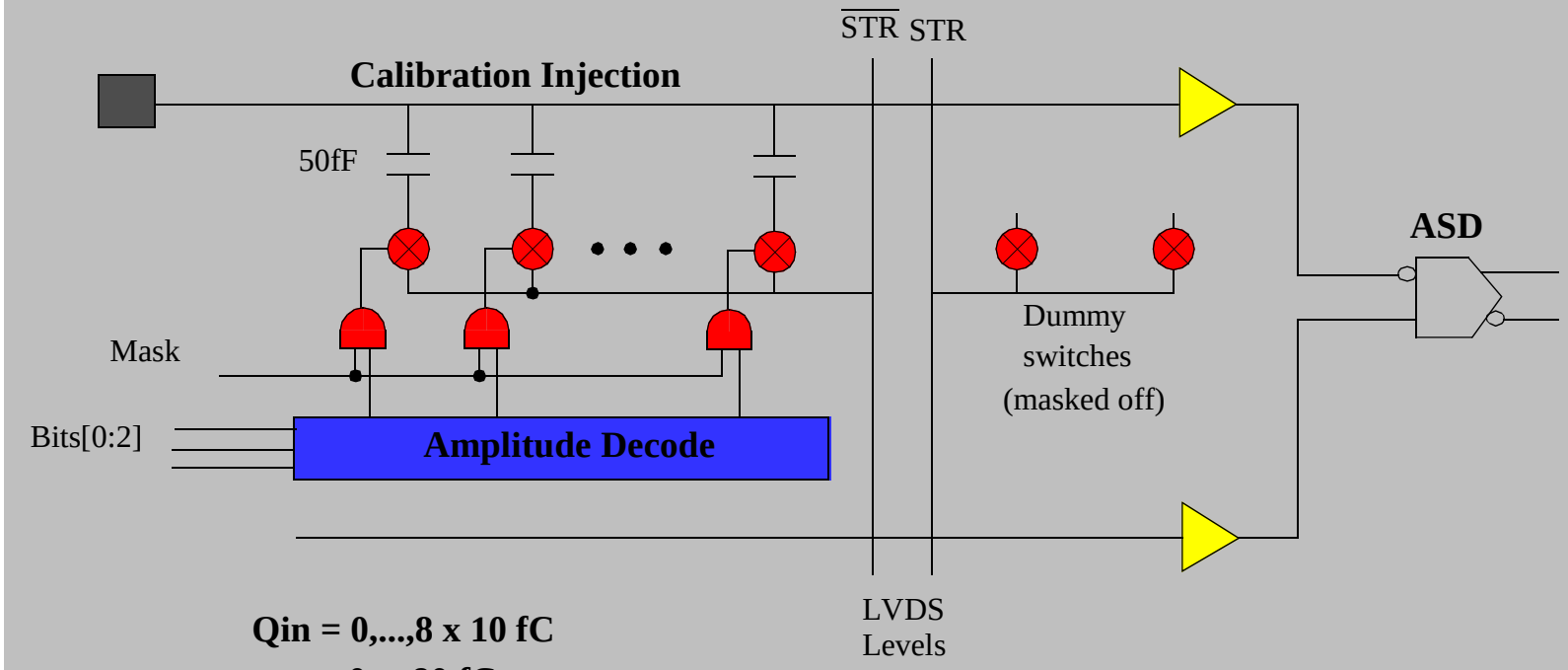
- Initialization data volume/CSM
  - CSM FPGA code ~ 2Mbits at powerup and after SEU detection
  - CSM setup constants ~ 50 bits at powerup, option changes, and SEU
  - ASD/TDCs (max count) ~ 6300 bits for largest chambers at powerup and SEU
  - TTCrx ~ small bit string at powerup, calibration, and option changes
- FPGA at PowerUp
  - All CSMs in parallel only seconds at 0.5 Mhz JTAG rate
  - In series (not OK) 80 minutes - some amount of parallelism needed
  - CSM & TDC constants - time small but sequencing can't be sloppy
  - TTCrx - time small
- SEU recovery time small (~ few ms for single unit - resync)

Calibration via TTC System

- Provisions in TTC system
  - B channel commands provide for calibration - addressable by TTC/CSM.
  - Can use the second TTC clock phase to give 104ps fine edge timing.
  - Can use Inhibit(0-3) (position in orbit to pulse) for course timing.
  - The TTC system has 4 triggers(0-3), one L1A from CTP and others for test.
- Sequence for test pulsing



Timing Calibration at the ASD (John Oliver)



Qin = 0,...,8 x 10 fC
= 0,....80 fC

$Q_{threshold}$ = 5 fC

Calibration pulse time constant ~ 0.1ns (to 20%) *i.e.* "Delayless"

Note: Must hide return edge of calibration pulse or place it out of time

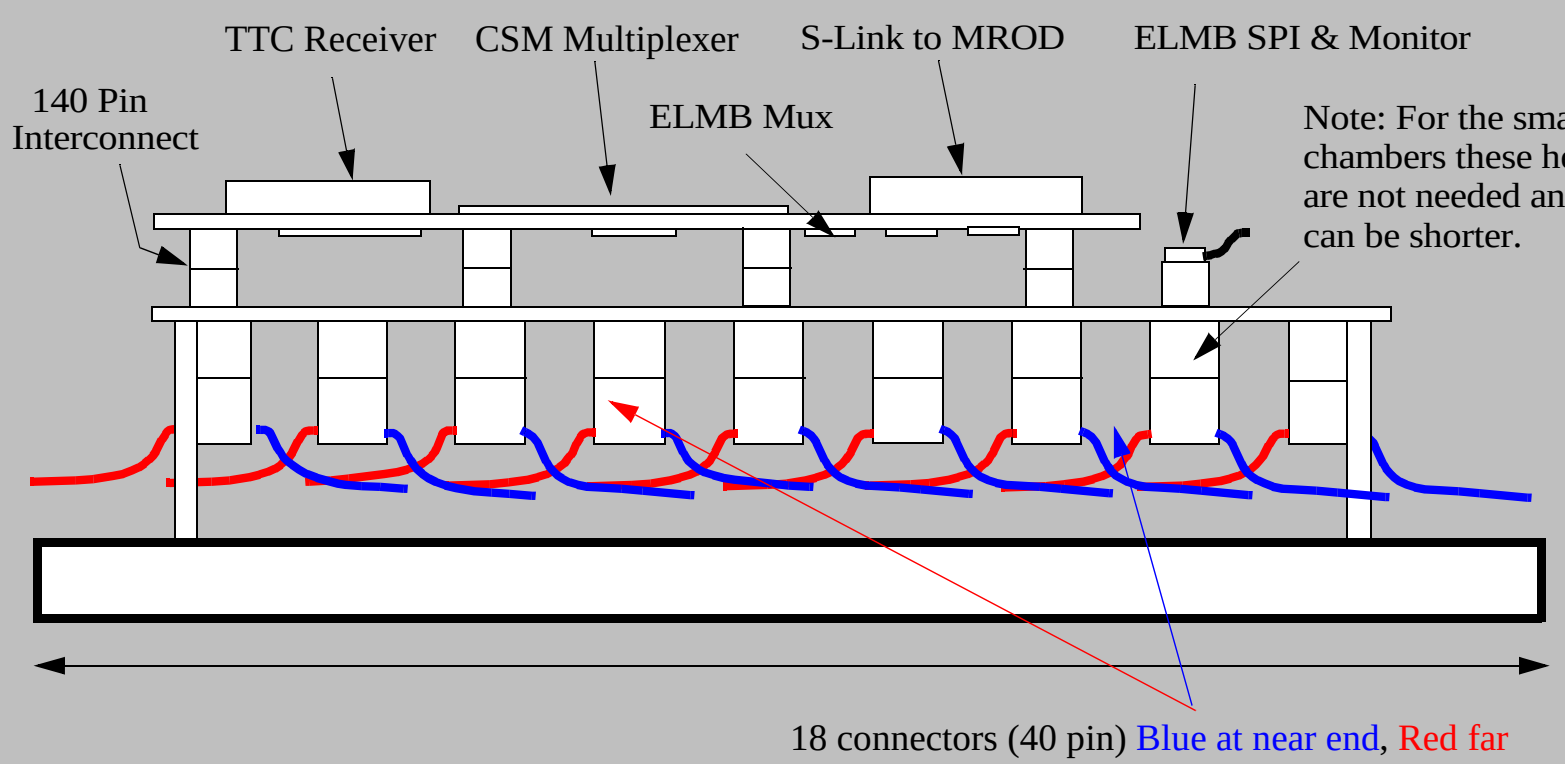
Timing Delay Issues

- Within ASD & TDC precise timing exists
- From ASD to TDC variations due to trace lengths are small
- Mezzanine card to mezzanine card timing uncertain to few ns
  - cable delay from CSM to mezzanine for pulse ~ same as for 40Mhz clock
  - uncertainty due to circuit variations for LVDS drivers/receivers & injection
  - calibration gives 23 numbers for each mezzanine card
- Tube data has trace differences on hedgehog boards
  - differences can be a few ns but will be fixed over time and can be calculated
- Conclusion - absolute times to few ns, relative in TDC OK!

CSM to MROD Fibre Path

- Requirement is ~90MByte/sec (32bits @ 22.5MHz)
  - S-Link option possible (radiation tested version ~ 5 watts at 5 volts).
  - New HP G-Link is low power and not radiation tested (3.3 volts).
  - Need 3.3 volt unit - CSM/ASD/TDC regulates 4 volts to 3.3 volts.
  - New unit can be run at 53.3MHz for 16 data bits (32 bits at 26.7MHz).
  - Baseline - use straight G-Link simplex protocol @ 53.3MHz.
  - Unit does 17 bits at up to 70Mhz (use 17th bit as high-order/low-order flag)
  - Radiation test all fibre components with the Virtex-E FPGA (Xilinx). For completeness include the G-Link receiver in test even though the receiver will not be in the radiation environment
  - More on radiation testing later

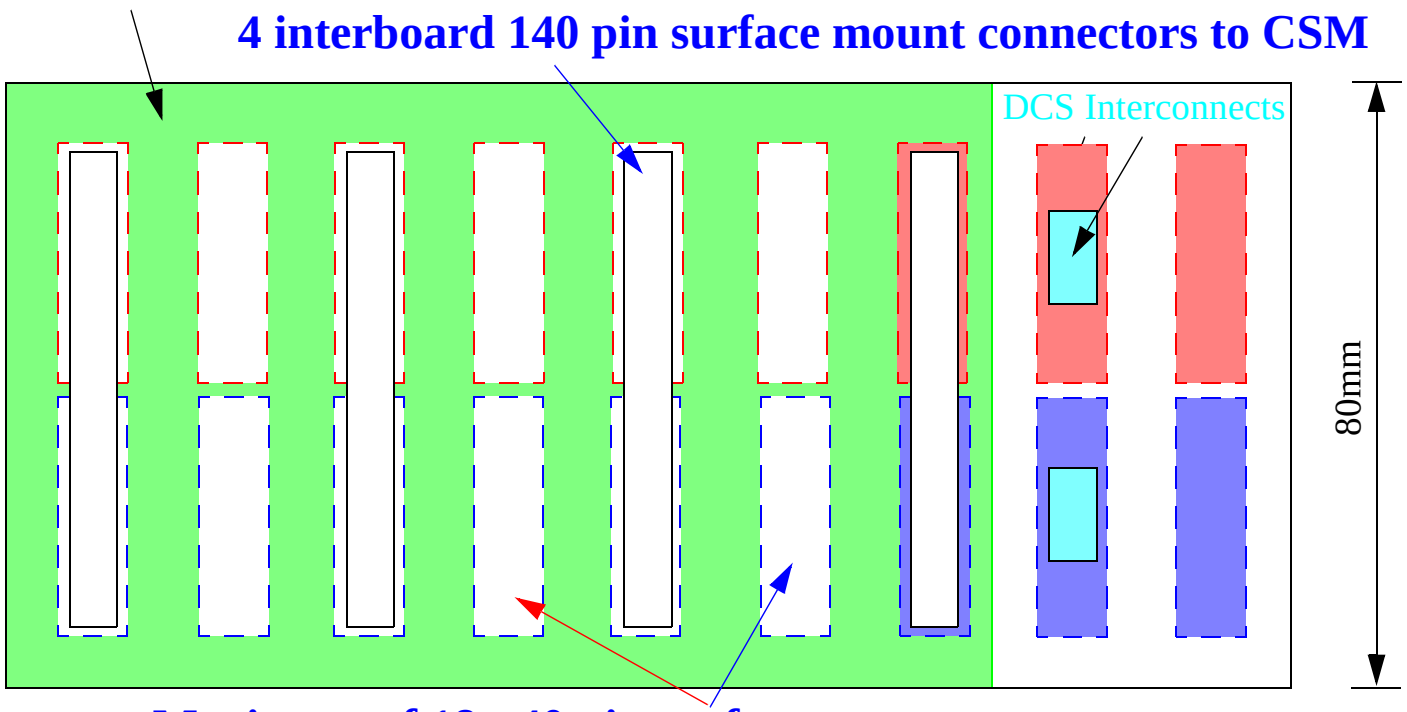
CSM Interconnect



Note: ELMB Mux is copy of 64 channel DCS mux

- Key items 4 x 140 pins to CSM OK; ELMB & Mux SPI OK

Cross Plate Motherboard for CSM Interconnect



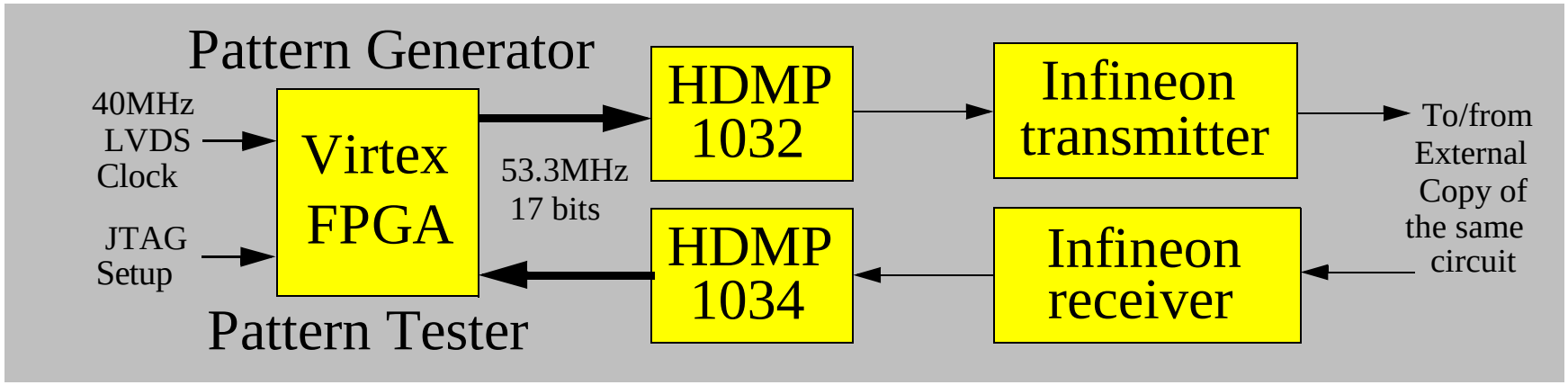
Note: DCS interconnect placed under CSM for short board & shaded 40 pin connectors deleted

Signal Counts

- Mezzanine to CSM Motherboard x 18 max
  - 8 JTAG (LVDS), 8 Data/CLK (LVDS) = 16 lines
  - 8 Analog PWR, 8 Digital PWR, 6 Sense, 2 Calibration = 24 + 16 = 40 lines
- CSM to CSM Motherboard - 3 x 140 pins = 420 pins
  - 8 JTAG (LVDS), 10 Data/CLK (LVDS) x 18 mezzanine cards = 324 lines
  - 6 Sense, 8 Digital PWR, 8 ELMB PWR = 22 + 324 = 346 lines
- ELMB Mux to CSM Motherboard
  - 6 Sense x 18 Mezzanine cards, 6 Sense x 1 CSM = 114 lines
  - 8 Digital I/O, 10 ELMB SPI = 18 + 114 = 132 lines
- Conclusion - it works with spare pins (dense with traces!)

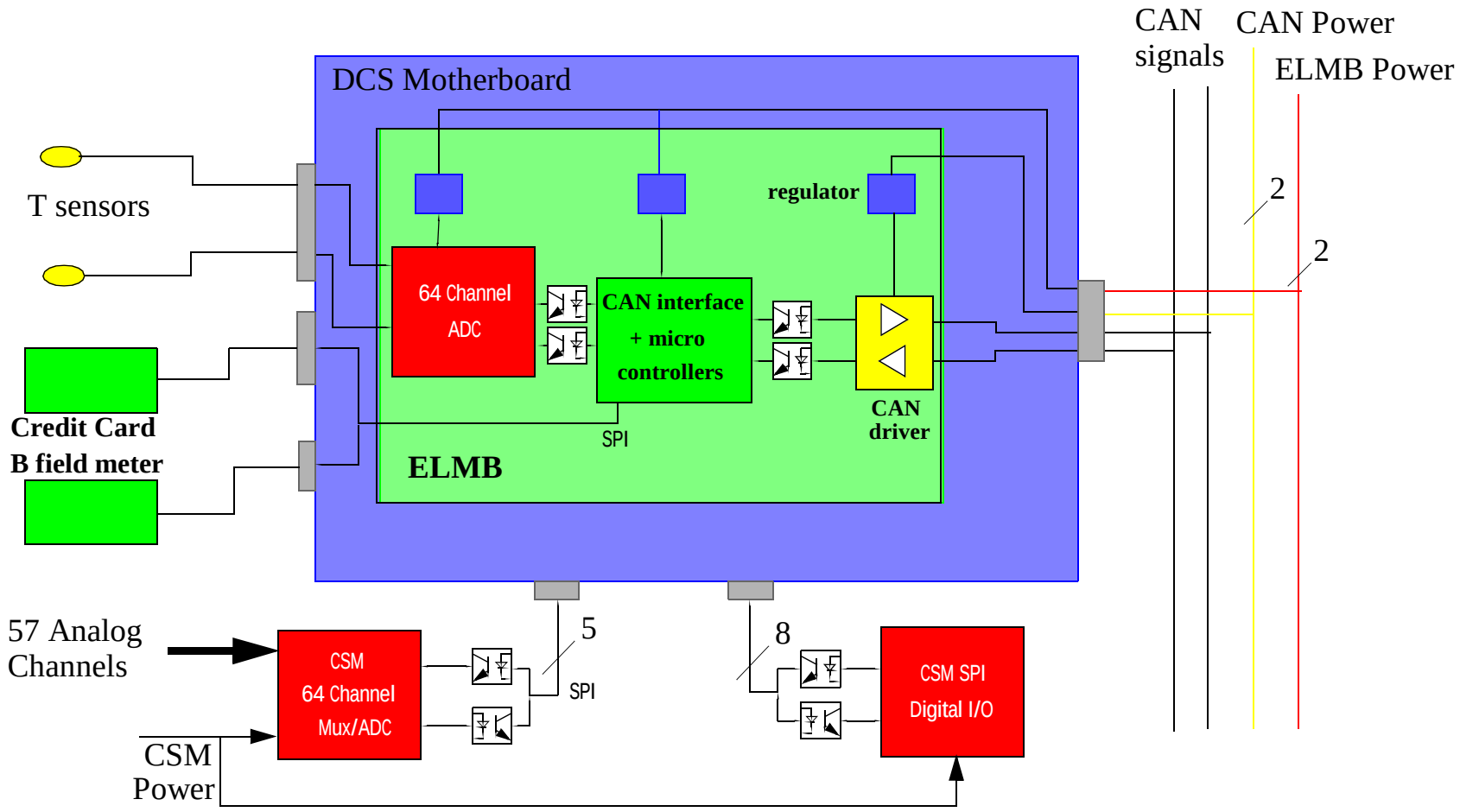
G-Link Test Fixtures

- G-Link encoder chip (HDMP-1032 & HDMP-1034)
- Optical transceiver Infineon (V23818K305V17)
- Xilinx Virtex XCV50E-FG256C (capable of LVDS I/O)
- 4 volt to 3.3 volt regulator (as used on Mezzanine card)
- 4 volt to 2.5 volt & 1.8 volt with same series regulators



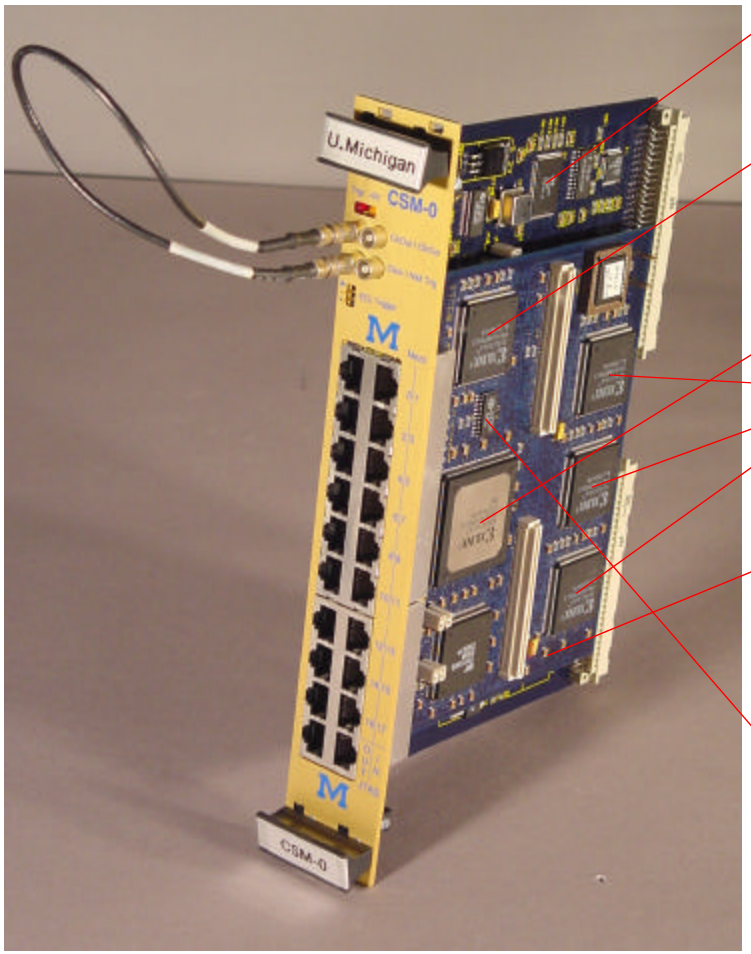
Monitoring the Data Acquisition Path

- The connection to the DCS system



What's Different from the Prototype?

Existing CSM-0 Module



FIFO → G-Link/S-Link to MROD

1 28mm FPGA → 1 10mm TTCrx + receiver

1 40mm FPGA → 1 17mm FPGA

3 28mm FPGAs → 2 17mm FPGAs

115 x 166mm board → 80 x 130mm

LVDS on VME → LVDS FPGA

Event Building → Time Division Mux

Clock Fanout → In FPGA DLL

Summary

- Basic design has been validated
- Miniaturization, JTAG, & optical output needed
  - Dense motherboard routing for mezzanine card connection
  - DCS multiplexer copied onto CSM backside
  - Remove event building in favor of time division multiplexing
  - Design and certify optical output
  - Initialize via JTAG
  - Add JTAG controller to FPGA
- Radiation test all components on CSM
- Refine the design for minimum of single point failure modes