

# ATLAS MDT Electronics PDR

## Mezzanine PC Board Design

### 1. General Description

The Mezzanine PCB contains the ASD ICs and AMT TDCs for 24 MDT drift tube channels. It makes the critical transition between the low-noise inputs at the preamplifiers and the digital, synchronous TDC outputs, and is thus a key part of the design. After several prototype designs and extensive testing, we have arrived at the design described here, which comfortably meets ATLAS specifications.

We have built (as of this writing) about 2500 channels of a pre-production mezzanine PCB we call **Mezz Lite**. This design uses an **ASD Lite** which has all key analog features of the final ASD but no on-chip programmability. Differences between Mezz Lite and the production design will be noted where appropriate.

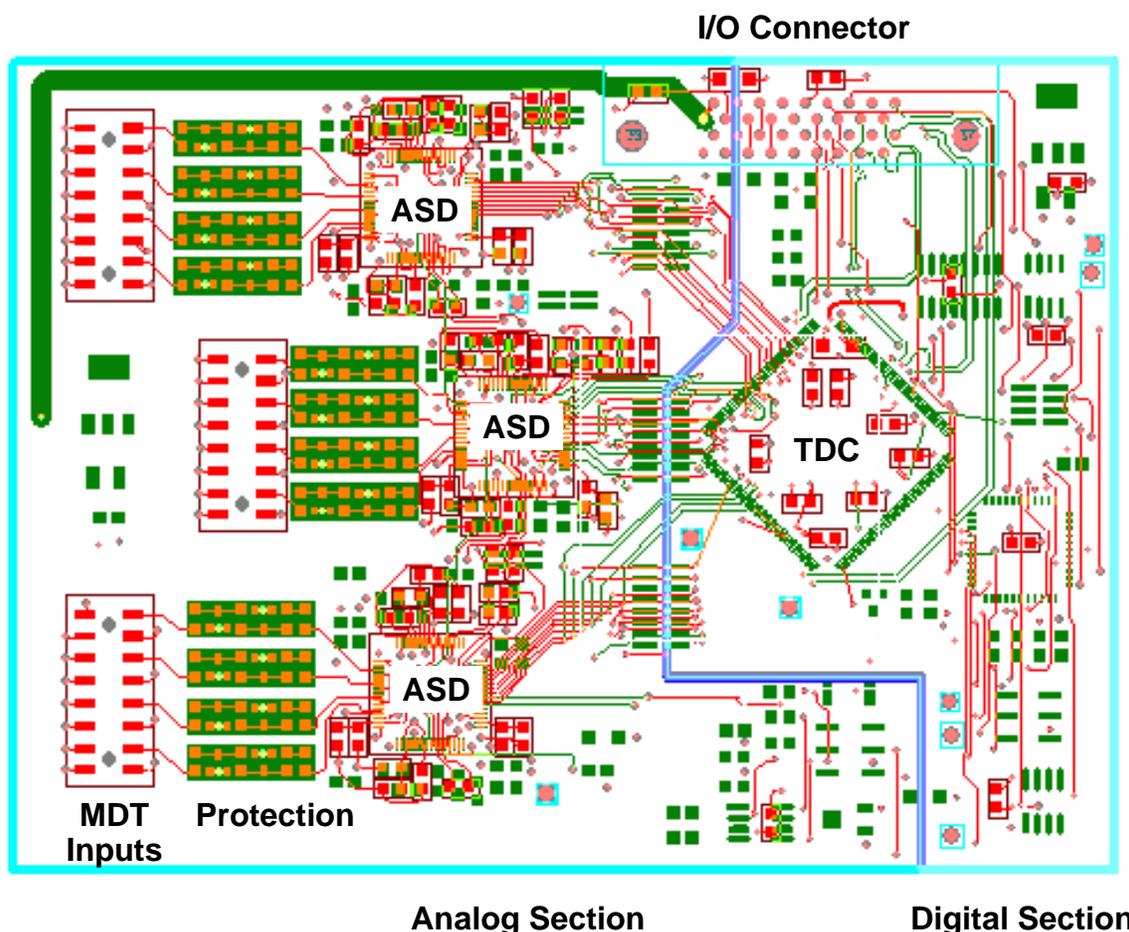


Figure 1 - Mezz Lite PCB Layout

The mezzanine board (Figure 1) is divided into separate analog and digital sections (both logically and physically). Other than the low-level pre-amp inputs, all I/O is LVDS. Analog and digital unregulated power are supplied separately. The *analog* section (left) contains input ESD protection, ASD chips, a voltage regulator, and (for Mezz Lite only) a DAC and buffer circuitry for discriminator threshold

programming. The *digital* section (right) contains the AMT TDC and a voltage regulator. On Mezz Lite there is also a Xilinx FPGA and LVDS drivers and receivers.

A block diagram of the mezzanine PCB design is shown in Figure 2.

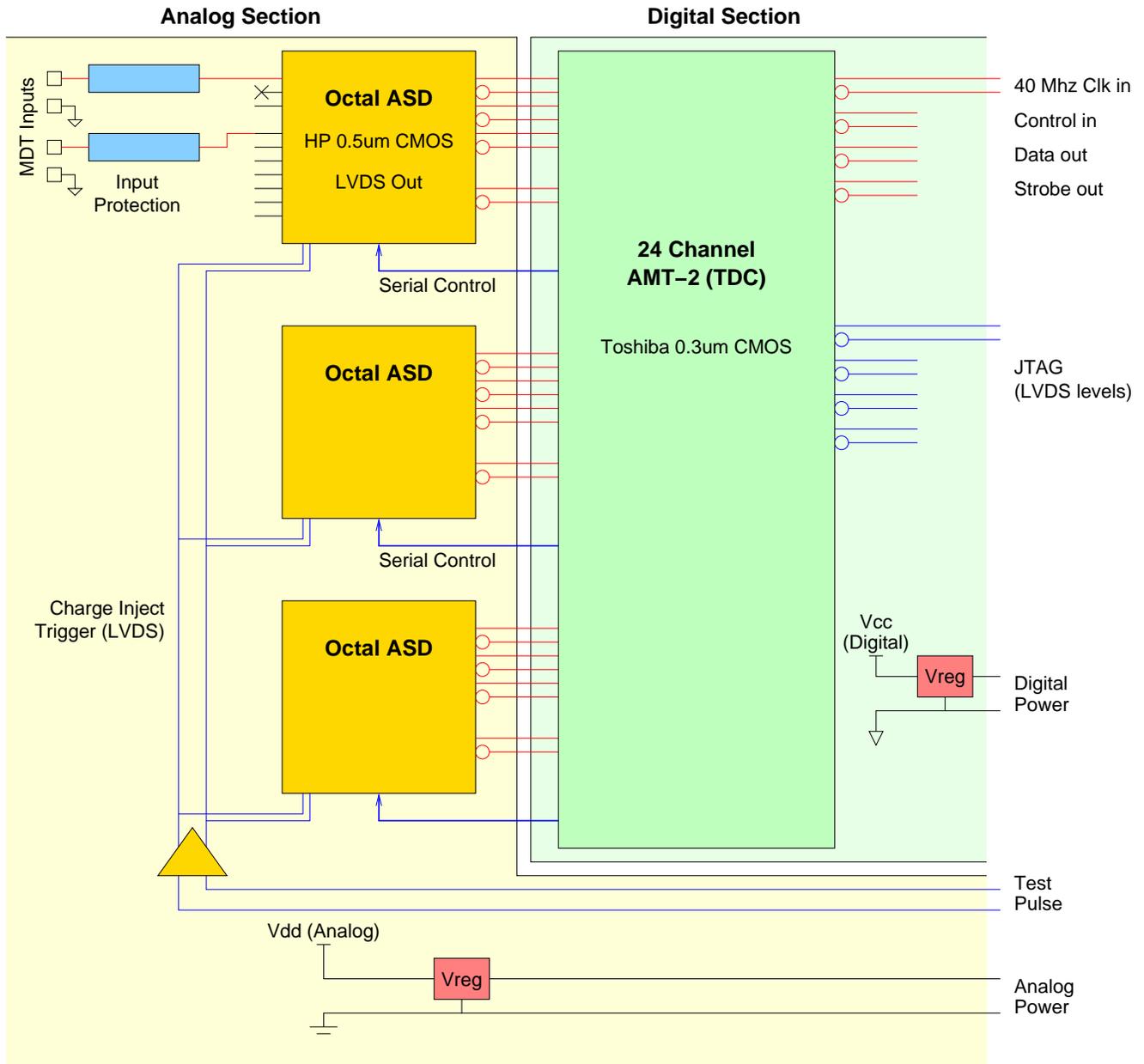


Figure 2 - Mezzanine PCB Block Diagram

## 2. Circuit Design

### 2.1. MDT Signal Inputs

The low-level MDT signals are carried on short PCB traces from a 0.1 inch pitch header connector on the bottom of the mezzanine PCB through a **protection circuit** to the ASD input pins. Each ASD input is protected against ESD and tube discharges by the circuit shown Figure 3.

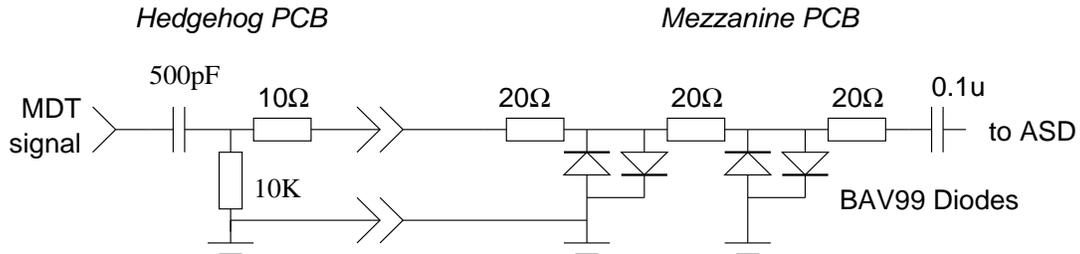


Figure 3 - Input Protection Schematic

The circuit consists of components on both the hedgehog and mezzanine PCBs. The circuit is essentially two sets of back-to-back diodes to ground, with series resistors. There is an additional series resistor before the ASD input which helps to limit the current in the on-chip ESD protection. On the hedgehog, the 10K resistor serves to maintain a DC potential of 0V in the remainder of the protection circuit. The 10 ohm series resistor (thru-hole, with fairly long leads) on the hedgehog PCB, plus the relatively long traces on the board form an R-L combination which somewhat attenuates very high frequencies. This reduces significantly the peak current through the first set of diodes if an HV discharge occurs. The second resistor-diode combination further attenuates the discharge signal.

We made measurements of a similar circuit on a test fixture, and found that each resistor-diode stage attenuated a simulated discharge signal by about a factor of 10. Thus, for a 3kV spark, the signal across the first set of diodes was about 300V, while the signal at the second set is about 30V. The attenuation is in practice somewhat greater in the first stage due to the long PCB traces on the hedgehog PCB.

The above description applies to the existing Mezz Lite design. The ESD protection has been significantly changed (improved, hopefully) on the final ASD, and we must still do extensive testing to be sure that the final system is robust against HV discharges.

Each ASD channel has in addition to the active input a **dummy input** which is bonded to an adjacent package pin. This dummy input is identical to the active input, with a fully functional pre-amplifier connected, and the two preamplifier signals are differentially amplified. The dummy pre-amp provides DC balance and rejection of substrate- and power supply coupled noise. It was determined empirically that further extending the dummy input back to the signal source did not improve performance.

The input signal traces are kept as short as possible to minimize stray capacitance, and parallel runs are avoided.

### 2.2. ASD Power Supplies

The ASD chips are entirely powered from the analog 3.3V on-board regulator. However, each ASD has 5 separate sets of power supply pins: pre-amp, shaper, discriminator, LVDS output / logic and analog pad driver. The CMOS N-Well and substrate contacts are provided with separate bonding pads for each of the four supplies in addition. On Mezz Lite these are connected as shown in Figure 4, with an RC filter on each power supply pin. This provides not only power supply filtering but also additional isolation

between the substrate and well contacts in each section due to the bond wire and package inductance. This configuration results in unconditionally stable operation with low crosstalk (< 1% to neighboring channels). We may find that on the production mezzanine board that this conservative design can be simplified somewhat.

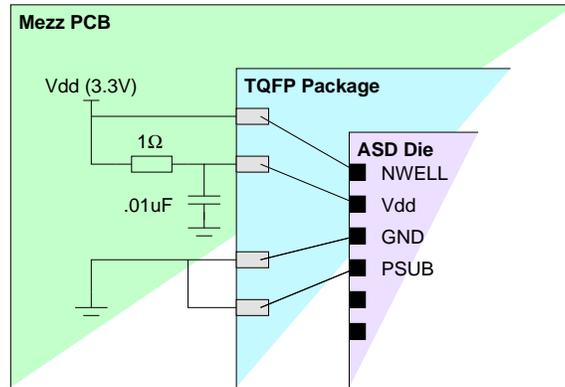


Figure 4 - ASD Power Supply Connections

### 2.3. ASD Control / Bias

The ASD Lite has several external connections to provide bias and set the operating conditions.

The **pre-amp/shaper bias voltage generator** is a self-biasing circuit on the ASD which provides 4 reference voltages which are used throughout the analog chain. The bias generator is bypassed as shown in Figure 5. The bypass capacitors return to the on-chip power supplies via dedicated bonding pads, and no external connections are made to the PC board power nets. This provides optimal power supply noise rejection. An optional external bias resistor may be used to adjust the bias voltages (currently not used).

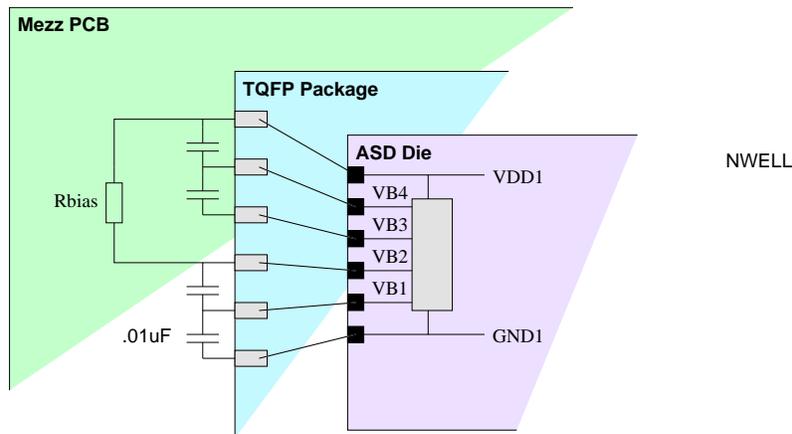


Figure 5 - ASD Bias Generator Connections

The timing discriminator thresholds and hysteresis are set externally on Mezz Lite. A JTAG-controlled DAC and op-amp circuit is used to set the thresholds on Mezz Lite. Since all threshold and hysteresis settings are programmed on-chip in the final design, the details of the Mezz Lite circuit will not be described here.

## 2.4. Test Pulse Injection

Test pulses of programmable amplitude may be injected into individual ASD inputs for testing. The selection of channels and pulse amplitudes is programmed via JTAG on the ASD. An external LVDS trigger signal is provided to each ASD. This signal will be provided from the CSM, and ultimately time-referenced to the LHC TTC (Trigger, Timing, Control) system. An LVDS buffer may be provided on the mezzanine card design. The details have yet to be determined.

No test pulse injection is provided on Mezz Lite.

## 2.5. ASD Outputs

Each ASD provides one LVDS pair for each channel. These signals are routed directly to the AMT TDC. Termination in 100 ohms for each pair is provided within the AMT. A 0.05 inch pitch test header is provided to give access to all ASD outputs for testing. Since the traces are quite short, no attempt was made to control their impedance. However, the two traces in each pair are routed parallel to each other, and equal length within pairs is closely maintained.

## 2.6. Digital Section (TDC)

On the production mezzanine PCB, the only active component in the digital section will (we hope!) be the AMT TDC. It provides two interfaces: a high-speed serial trigger/clock/readout interface which operates during data acquisition, and a low-speed serial JTAG interface which is used only for initialization and control. The JTAG interface is not active during data acquisition and requires no special care in implementation. The high-speed serial interface operates continuously, and considerable care was taken to minimize feed-through to the analog circuitry.

The Mezz Lite contains a Xilinx FPGA which implements the JTAG state machine. This will be eliminated for the final mezzanine PCB design.

# 3. PCB Layout

The Mezz Lite PCB design is a 6-layer multilayer design, separated into analog and digital sections. Two somewhat different Mezz Lite PCB layouts exist and are in production. The first variant (for 3x8 tube geometry) was designed by the author and will be described in detail. The second variant (for 4x6 tube geometry) is not described here but detailed layout drawings are included. Performance of the two variants is similar.

The 3x8 Mezz Lite layout is shown in Figure 1. The figure represents a combination of top- and bottom-side components for completeness. The MDT inputs are received from the hedgehog PCB via 0.1 in. pitch header connectors on the solder side of the PCB. Signals flow to the right through input protection circuits and ASDs (both sides) to the AMT TDC. All I/O is via a multi-pin 0.025 in pitch connector.

## 3.1. Input Protection

A detail of the input protection circuit layout is shown in Figure 6.

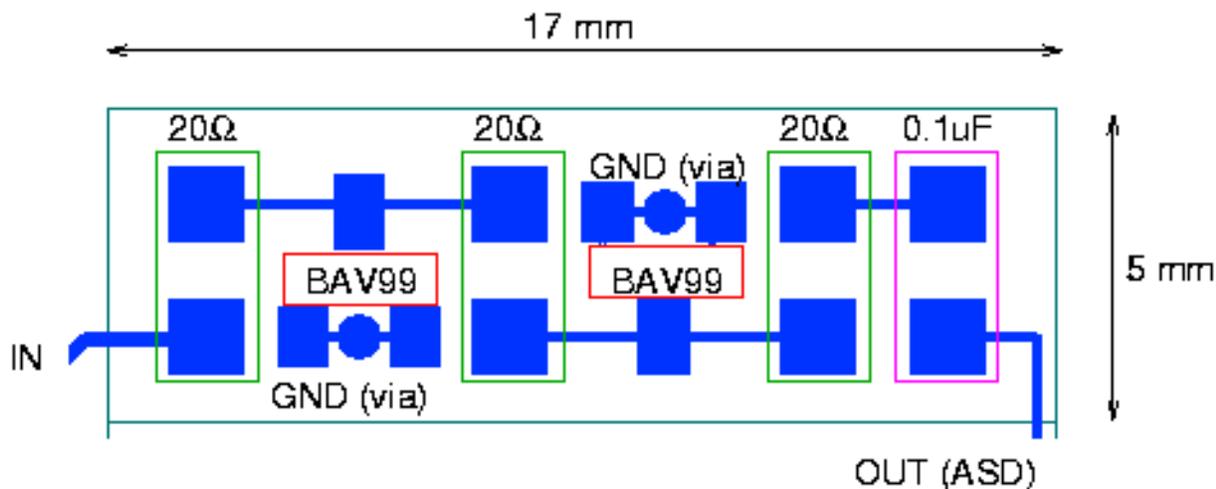


Figure 6 - ASD Input Protection Layout

Note the compact overall layout. Particularly important are the very short ground connections to the diodes. We experimented with many different physical configurations for the layout of the protection circuit, and found that component lead lengths of even a few mm would substantially degrade the performance of the protection circuit. The layout shown has been demonstrated to protect an ASD Lite chip against repeated simulated tube discharges caused by shorting the terminals with a screwdriver.

The entire layout is not covered by solder mask, to permit the addition of high-voltage conformal coating over the protection circuit.

### 3.2. Layer Structure

As shown in Figure 1, the Mezz Lite PCB layout is separated into analog and digital sections. The layer structure is shown in Figure 7. In the **analog section**, two analog ground layers are located immediately under the analog components to provide a short, low-noise current return path for the analog signals. Analog power is distributed on a dedicated plane. An inner signal layers is used for signal routing in a few congested areas. In the **digital section**, two grounded shield planes are located immediately inside the signal layers. All high-speed digital signals are routed on an inner layer between these two grounded planes, to minimize crosstalk to the analog section. Digital power is distributed on the inner signal layer.

Analog	Layer Stacking	Digital
1 - - - Signal (top)		- - - Signal (top)
2 ——— AGND		——— Shield (DGND)
3 ——— AVdd		——— DGND
4 - - - Signal (inner)		- - - Signal / DVdd
5 ——— AGND		——— Shield (DGND)
6 - - - Signal (bottom)		- - - Signal (bottom)

Figure 7 - Mezz Lite PCB Layer Structure (3x8 topology)