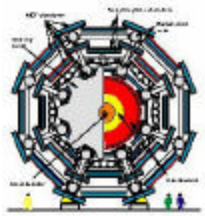

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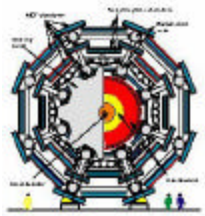
Preliminary Design Review - 22 Feb 2001

• System specifications and overview	J.Oliver	25’
• High Voltage Hedgehog Cards	A.Lanza	20’
• Signal Hedgehog Cards	E.Spiriti	10’
• Octal ASD - Specification, design, performance	C.Posch	20’
• AMT/TDC - Specification, design, performance	Y.Aria	20’
• On-chamber architecture & design - Mezz-cards, f-cage, cabling	E.Hazen	20’
• CSM - Architecture, interfaces to ROD & DCS, performance	J.Chapman	25’
• System performance measurements	J.Guimaraes	20’
• The MDT-ROD (MROD)	A.Koenig	25’
• Radiation tolerance issues	R.Richter	20’
• Cost and responsibilities	G.Brandenburg	20’



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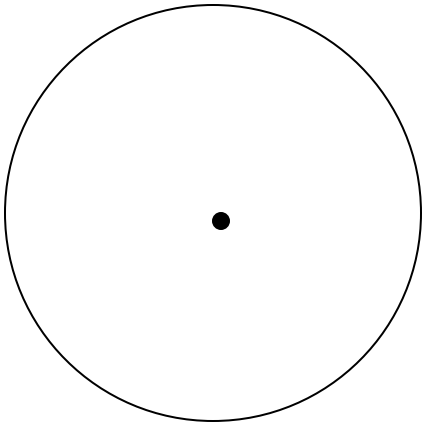
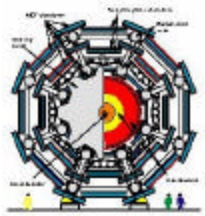
MDT properties & specifications



• MDT dia	30mm
• Anode wire	50μ tungsten /rhenium, 44 Ω /met
• Drift gas	Ar/CO_2 (93% - 7%) - Inorganic, superior aging
• Pressure	3 Atmospheres
• Gas gain	$2*10^4$ @ 3.1 kV
• Characteristic impedance	380 Ω
• Max drift time	~ 700 nsec
• Maximum length	6 meters, ~ (20ns one way propagation delay)
• Max background rate	400kHz (Mev) neutrons --> keV photons
• Single MDT resolution	~80 μ



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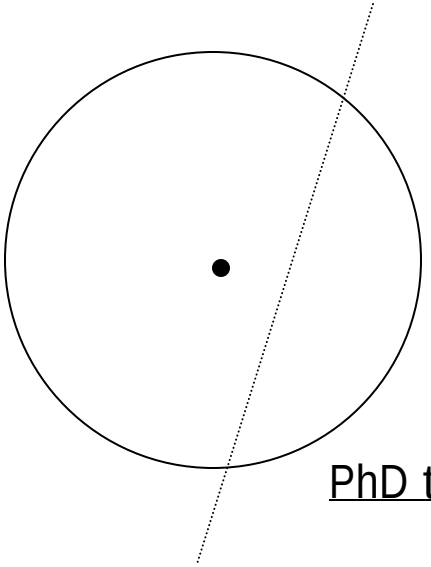
MDT signal formation

- Studies, simulations-



PhD theses;

W.Riegler, G.Viehhauser, ..

Other studies;

"Non-linear MDT Drift Gasses like Ar/CO_2"
M.Aleksa, W.Riegler

"MDT performance in a High Rate Background Environment"
M.Aleksa, M.Diele, N.Hessey, W.Riegler

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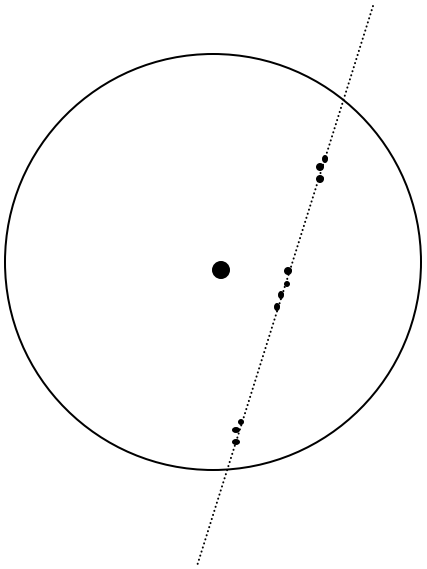
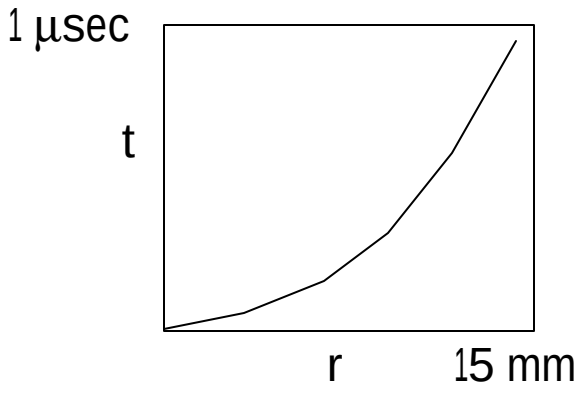
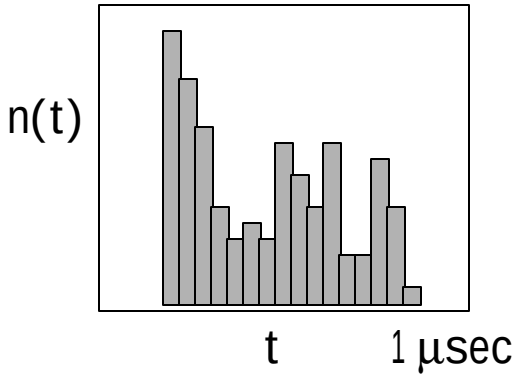
MDT signal formation - Key features



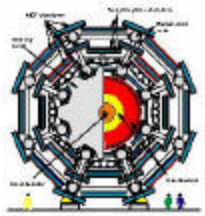
- Non-linear r-t relation



- Tail clusters are widely separated by non-linear r-t
- Late arriving clusters produce multiple (2-3) “fakes”



n(t)=no electrons/time at anode wire



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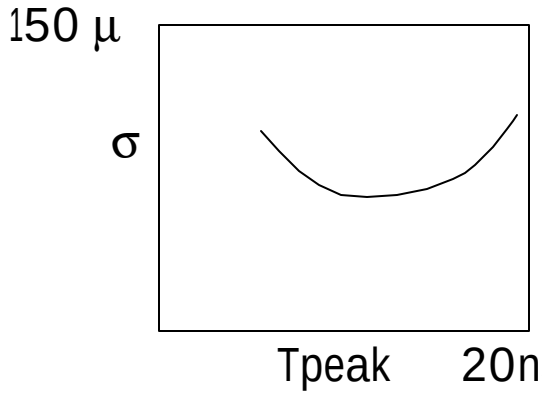
MDT Signal Processing Features

- 6 meter tube length --> 380Ω termination resistor

$$enc = e^{1}\sqrt{\frac{kT \cdot T_{peak}}{2 \cdot R_{term}}} =\sim 4500\_electrons\_rms@T_{peak} = 12.5ns$$

- Low noise favors ***shorter*** T_{peak}
- Good charge collection efficiency favors ***longer*** T_{peak} ($1/(t+t_0)$ pulse shape)
- Optimal peaking time 10ns - 15ns (simulations, W.Riegler)



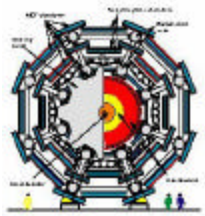
Note: Diagrams not to scale

- Primary electron charge collection efficiency in 12.5ns peaking time : ~7.5% (~1500 e/pe)

⇒ Thermal noise equivalent to ~4 pe (primary electrons) including preamp noise

⇒ Discriminator threshold ~ 5 σ = ~20 pe

- "Typical" muon track of order ~100pe (in leading edge)



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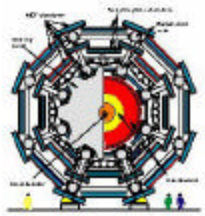
MDT Signal Processing (Con't)

- Preamp requirements
  - Zin small compared with 380 Ω for good charge collection ~$Z_0/(Z_0+R_{in})$
  - Zin ~ 120 Ω ok
  - Noise resistance small compared with 380 ohm (multiplier = sqrt(1 + Rnoise/Rterm))
  - Rnoise ~ 120 Ω --> e_n ~ 1.4nV/$hz^{1/2}$
  - Low power design (Power budget : 35mW/channel for ASD)
- High background rate (400kHz)

⇒ Must deal with errors due to baseline shift

⇒ Implies ***baseline restoration*** or ***bipolar shaping***

⇒ Choose ***bipolar shaping*** with Tpeak~12.5 ns



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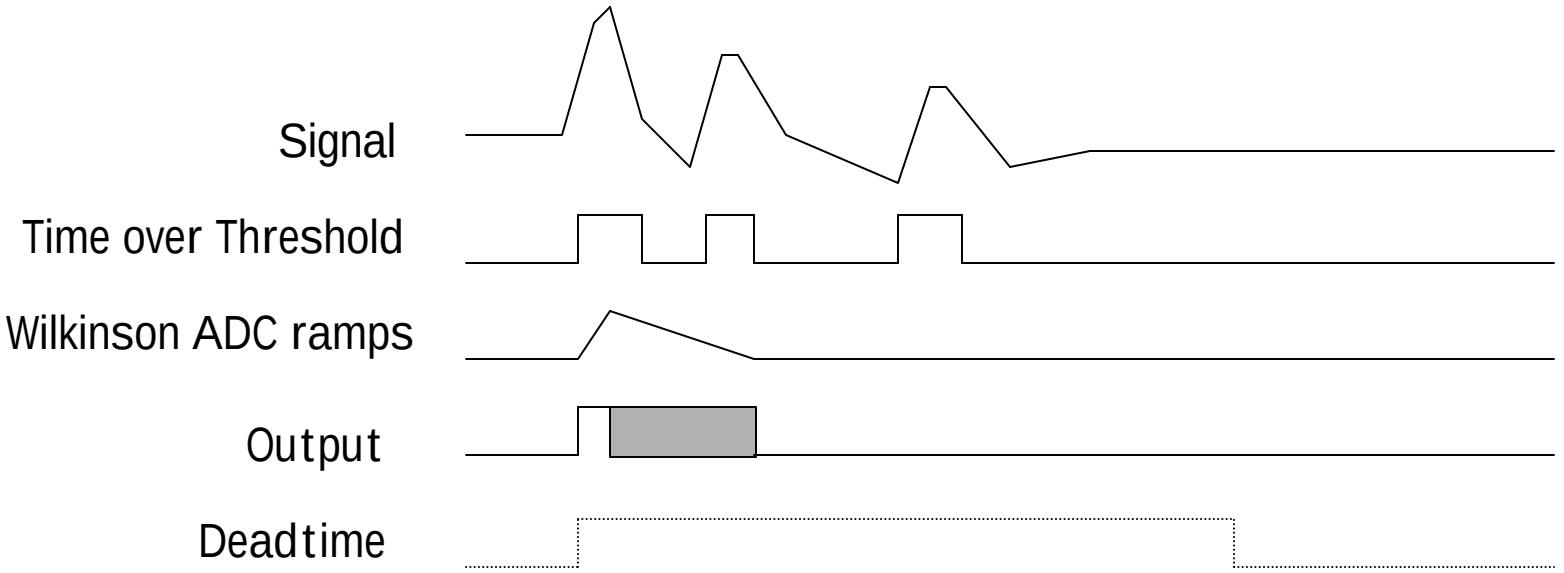
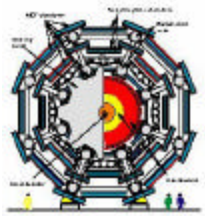
MDT Signal Processing (cont)

- **Time slew correction** : Pulse width encoded gated integrator (Wilkinson ADC)
- **Elimination of "fakes"** : Programmable dead time up to Tmax = 1 μsec
- **Compact design :** On-chip programmable features, DACs, etc
- **Technology choice :** HP 0.5μ "analog" CMOS





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MDT Signal Processing (cont)

- **Timing calibration**
  - ⇒ On-chip charge injection capacitors (3 bits, 50ff)
  - ⇒ "Near Zero" delay injection (***No logic gates*** in cal_inject path, $\tau = \sim 300$ps)
  - ⇒ Single strobe per mezz card allows calibration of timing differences
  - ⇒ Along with systematic timing effects (pc traces, etc) allows extraction of ***23 timing differences per mezz card***
  - ⇒ ***No absolute timing information*** required (or obtained)
  - ⇒ Autocalibration required between mezz cards (~15,000)

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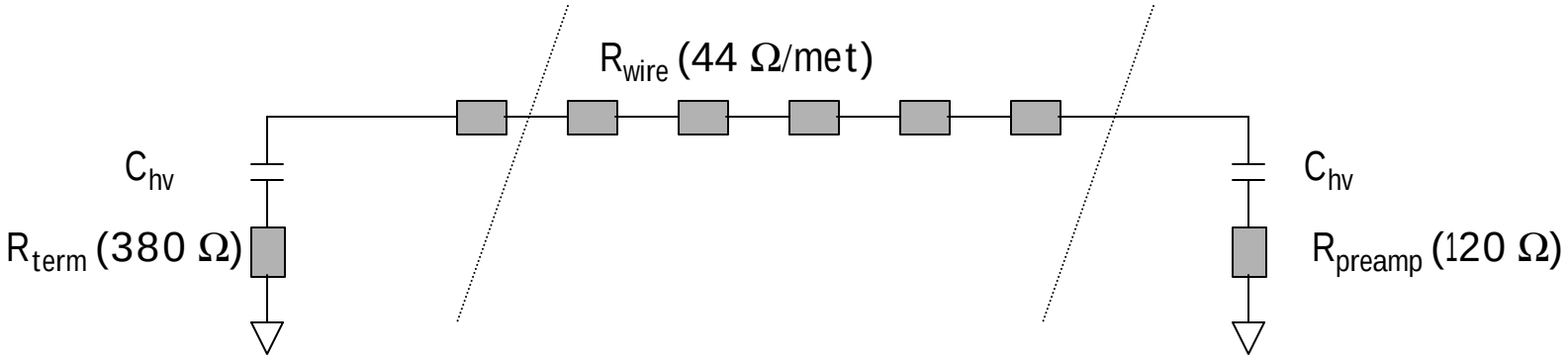
High Voltage Capacitors

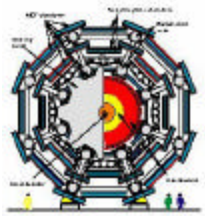
- Anode wire equivalent circuit.



- Wire resistance forms "undesirable" ***pole/zero network*** with other passive components

$$transfer\_function \approx \frac{1+sCR_{left}}{1+\frac{sCR_{total}}{2}}$$

- Differentiates ***near end*** pulses more strongly than ***far end*** pulses
- Effect is minimized by large Chv
- Large hv caps are "unpleasant" from esd, cost, physical size, etc.
  - ⇒ Chv ~ 500pf is compromise
  - ⇒ differentiation time constants > 100 ns



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Electronics Configuration

- HV dist & blocking components on “Hedgehog” cards --> Ease of chamber production
- Active components on Mezzanine Card --> Decouples Electronic and Chamber production
- Mezzanine card : 3x Octal ASD, 24 channel TDC, all active signals LVDS
- Small (fc) signals-->Full “hermetic” faraday cage required

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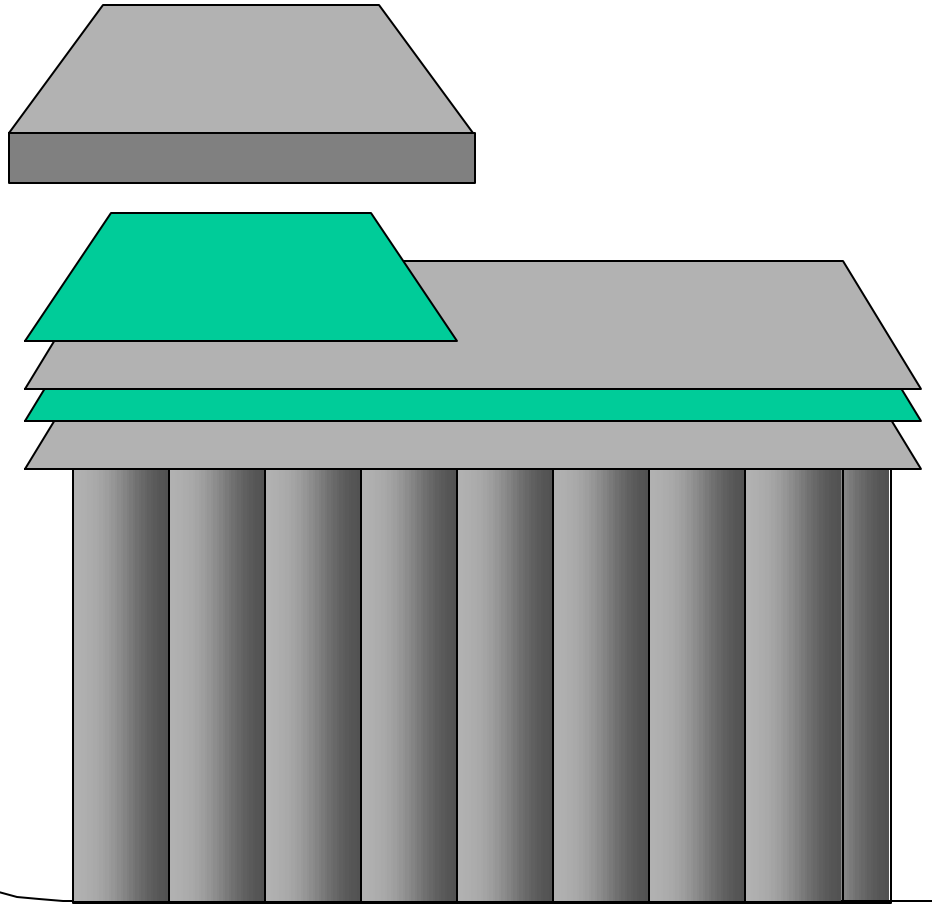
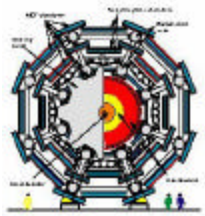
Electronics configuration



Mezzanine card enclosure

Mezzanine card (ASDs, TDC, i/o)

Faraday top plate (sides not shown)
Hedgehog card (passive)
Faraday bottom plate
24 MTD array : 3x8 & 4x6



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Other PCB Issues/Requirements

Signal Hedgehog

- 3.2 kV operation, 6kV components
- Low capacitance (Hi-Z) signal traces (noise, signal degradation & reflections)
- Low crosstalk - “widely” separated signal traces
  - ⇒ 2-layer design

Mezz Card

- ASDs, TDC, --> Mixed signal design
- Low crosstalk
- Robust esd/spark protection
- Low clock/digital feedthrough (few % above thermal)
- Maintain thermal noise levels (< 1 fc)
  - ⇒ 6 layer designs
  - ⇒ Split (Analog/Digital) power & ground planes
  - ⇒ LVDS for all “real time signalling”

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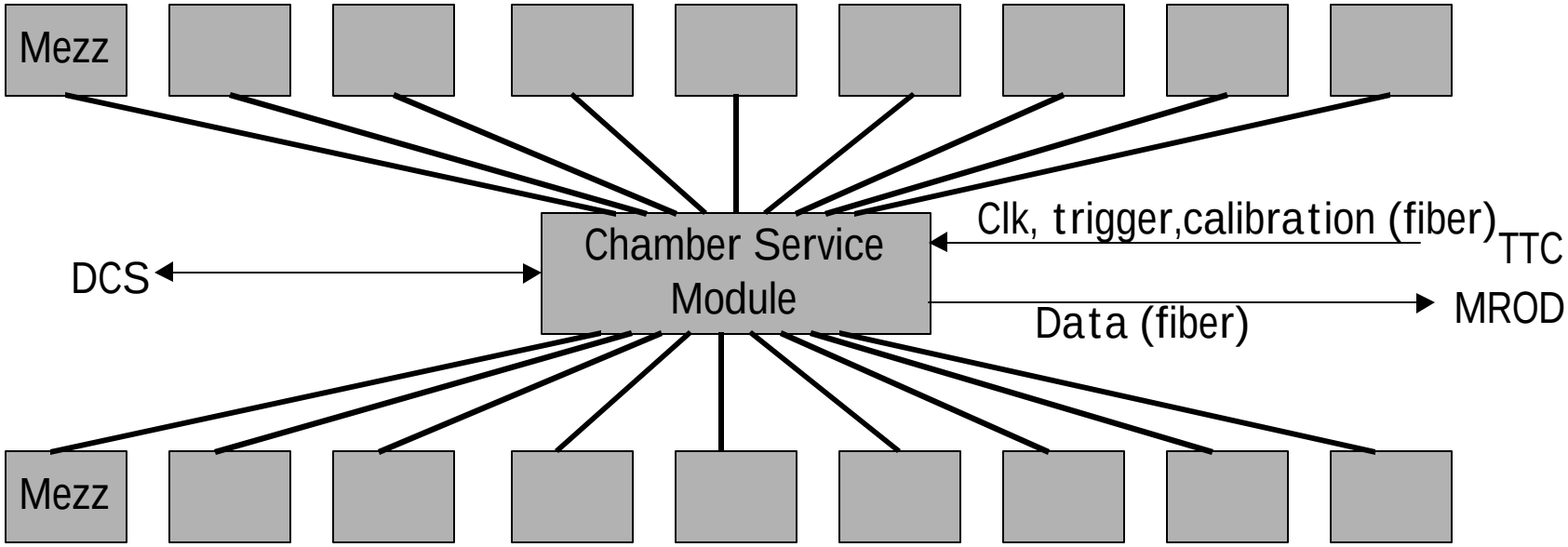
Finished MDT Chamber

- Connections to CSM -



40 conductor twisted pair ribbons carry :

- Power, Gnd
- Data
- Clk
- Timing calibration
- V,T monitoring

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Finished MDT Chamber

- Up to 18 HH and Mezz cards -