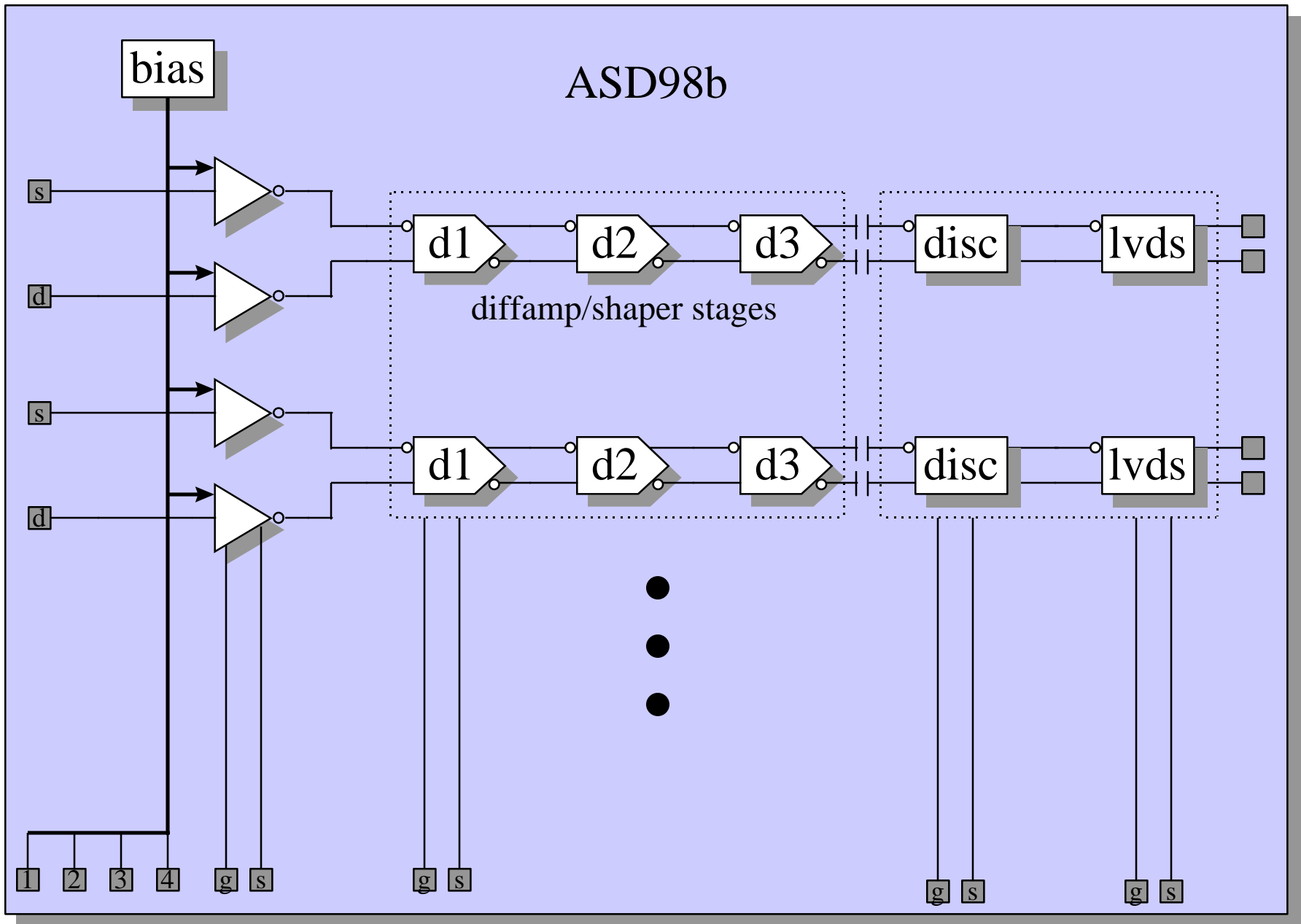


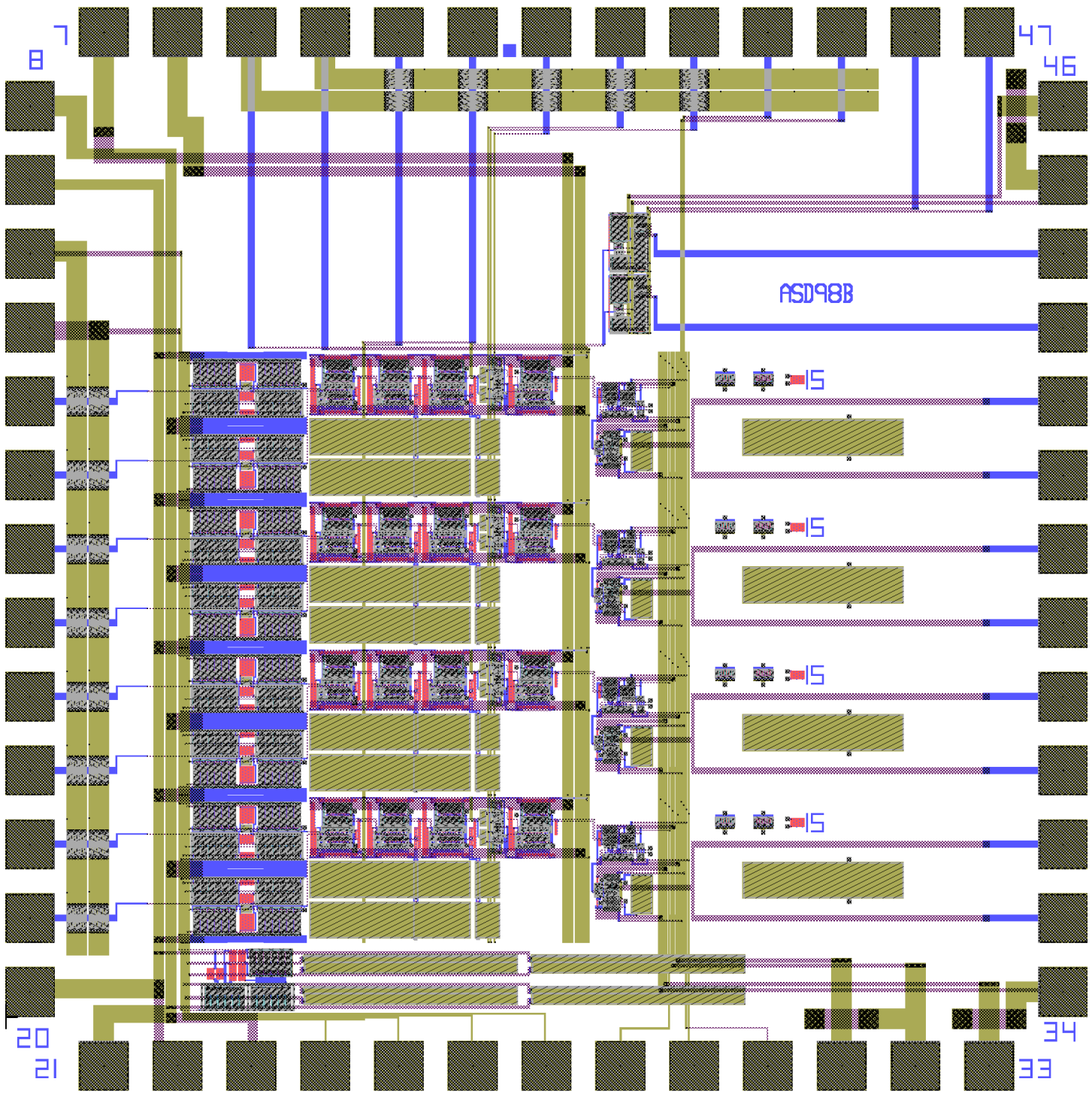
ASD Status Report

Nov. 1998

- ASD98b prototypes received ~ Nov. 1, '98 (0.5u HP CMOS @ 3.3v)
- Objectives
 - (a) Assured stability
 - (b) Crosstalk reduction
 - (c) ASD-lite prototype
- General features
 - (a) Four channels/chip
 - (b) Preamp $Z_{in} = 120$ ohms
 - (c) Standard tail cancellation shaping
 - (d) Disc + lvds output
 - (e) Analog out ch0 only

- New features
 - (a) Fully differential internal stages (stability)
 - (b) Modified bias circuit for lower PSRR (stability)
 - (c) No shared bias lines between preamp & shaper, disc, lvds (stability, xtalk)
 - (d) Separated ground and substrate connections (bond wire inductance/resistance) (stability, xtalk, substrate coupling)
 - (e) Chip on board packaging (optional) : ease of probing, best substrate decoupling





8

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ASD98B

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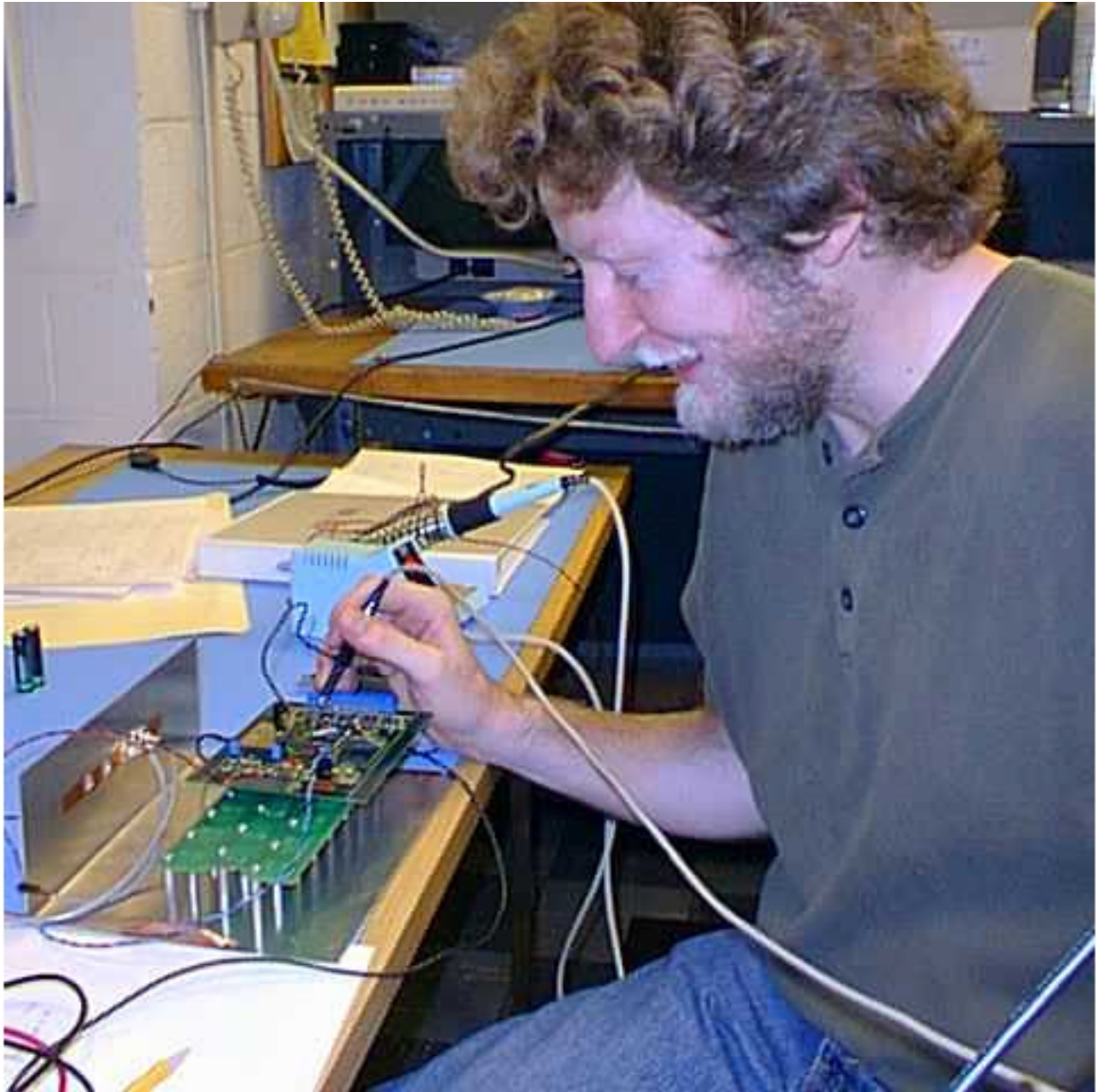
15

15

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34

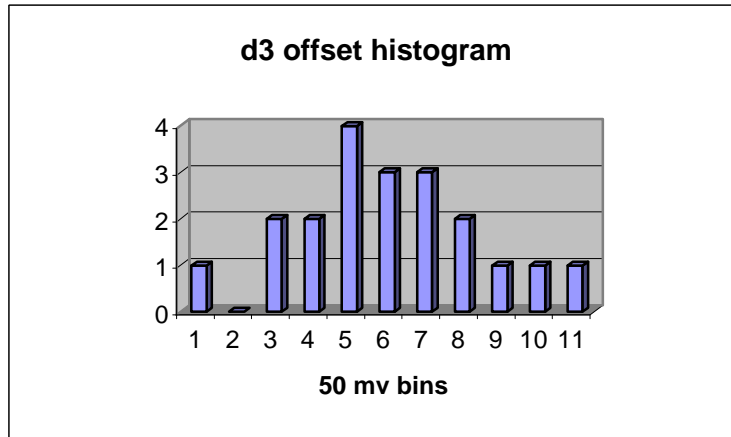
33



chip	channel	preamp	-da1	da2	-da3
1	0	3.6	-9.6	13.3	-22.8
1	1	5.93	7.5	-14.1	28.6
1	2	1.26	10.8	-25.3	57.7
1	3	1.51	17.7	12.9	-10.1
2	0	0.16	-0.2	3.3	19.8
2	1	1.16	-27.6	59.9	-115
2	2	1.3	2.2	-40.1	53.4
2	3	8.43	-47.1	107	-257
4	0	-1.82	36.7	-83	162
4	1	1.64	-15.3	34.3	-65.7
4	2	5.35	-24.4	54.8	-104
4	3	3.8	-14.5	40.9	-73.5
5	0	4.95	-33.8	63.2	-152
5	1	2.78	-27.8	43.1	-71.8
5	2	2.47	21.1	-11.4	47.2
5	3	-0.9	24.5	-24.4	110
6	0	-1.44	45.5	-87.2	207
6	1	2.98	-19.7	52.7	-56.9
6	2	-4.17	-1.16	10.2	-25.1
6	3	-1.13	-44.8	78.9	-181

Average 1.89 -5.00 14.45 -22.46
 Stddev 3.01 26.03 51.14 113.80
 SPICE Monte Carlo 5.00 41.00 85.00 148.00

Bin	Frequency
-250	1
-200	0
-150	2
-100	2
-50	4
0	3
50	3
100	2
150	1
200	1
250	1
More	0

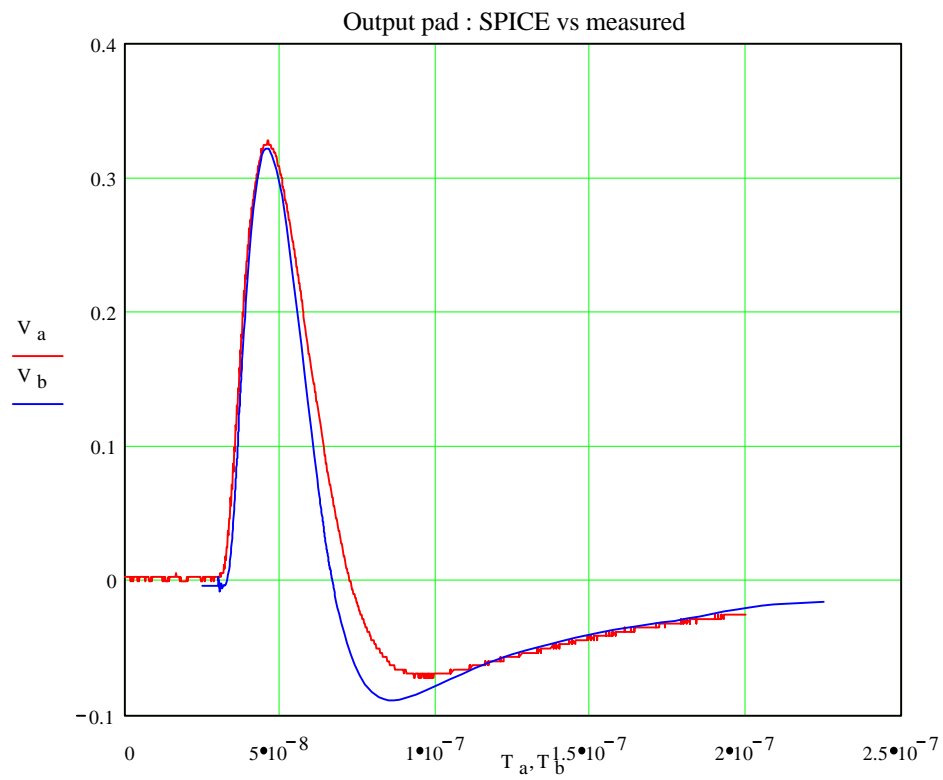


$T_a := \text{READPRN}(\text{"chip01.txt"})^{<0>}$

$V_a := \text{READPRN}(\text{"chip01.txt"})^{<1>} \cdot 10$

$T_b := \text{READPRN}(\text{"SPICE.txt"})^{<0>} + 25 \cdot 10^{-9}$

$V_b := \text{READPRN}(\text{"SPICE.txt"})^{<1>} - 1.7$



Zin

Extraction of input impedance from signal size vs termination resistor : simple current divider

sig := READPRN("Zin.txt") <1>

Z_t := READPRN("Zin.txt") <0>

i := 0.. rows(Z_t) - 1

Z _{t_i}	sig _i
100	341
200	481
360	597
510	622
680	659
820	675

$$\text{siginv} := \frac{1}{\text{sig}} \quad \text{ZtInv} := \frac{1}{Z_t}$$

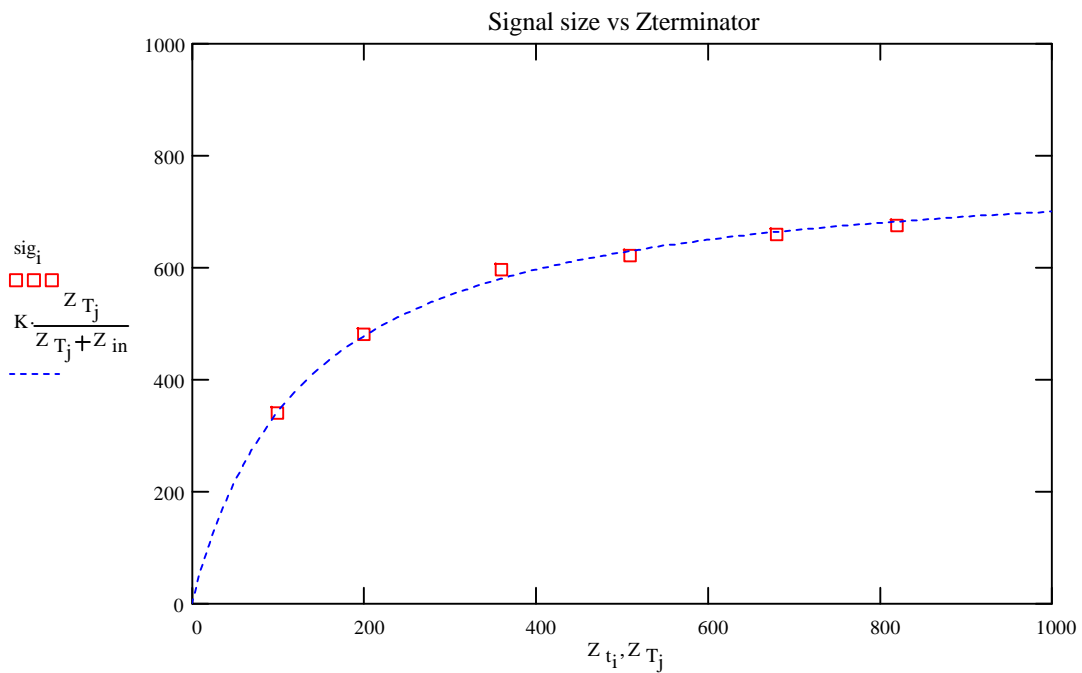
m := slope(ZtInv, siginv)

$$K := \frac{1}{\text{intercept}(ZtInv, \text{siginv})} \quad K = 792.229$$

$$Z_{in} := K \cdot m$$

j := 0.. 100 Z_{T_j} := j · 10

$$Z_{in} = 131.4$$

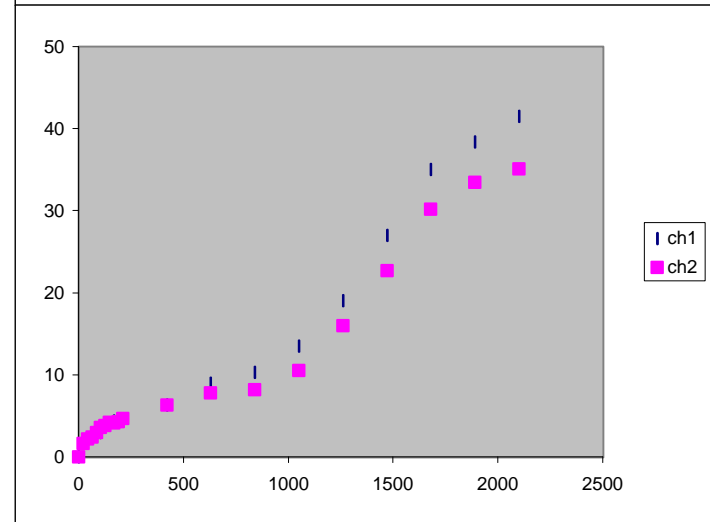
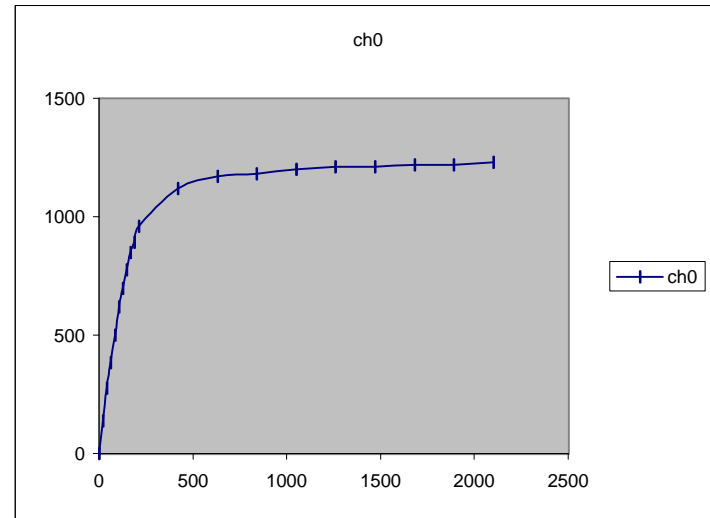


LVDS OUTPUTS		out	/out	Vcm	Vswing
chip04	ch0	1.173	1.336	1.2545	0.163
chip04	ch1	1.169	1.333	1.251	0.164
chip04	ch2	1.164	1.331	1.2475	0.167
chip04	ch3	1.156	1.326	1.241	0.17
chip01	ch0	1.163	1.323	1.243	0.16
chip01	ch1	1.163	1.324	1.2435	0.161
chip01	ch2	1.158	1.321	1.2395	0.163
chip01	ch3	1.15	1.318	1.234	0.168
chip02	ch0	1.17	1.333	1.2515	0.163
chip02	ch1	1.168	1.333	1.2505	0.165
chip02	ch2	1.163	1.33	1.2465	0.167
chip02	ch3	1.154	1.325	1.2395	0.171
chip05	ch0	1.177	1.324	1.2505	0.147
chip05	ch1	1.174	1.34	1.257	0.166
chip05	ch2	1.17	1.338	1.254	0.168
chip05	ch3	1.16	1.333	1.2465	0.173
chip06	ch0	1.17	1.331	1.2505	0.161
chip06	ch1	1.167	1.329	1.248	0.162
chip06	ch2	1.164	1.328	1.246	0.164
chip06	ch3	1.155	1.323	1.239	0.168
mean				1.247	0.165
sigma				0.006	0.005

Channel 0 to ch[1:3] crosstalk

	approx	2100	d3			
att factor	pe equiv	Qin(fc)	ch0	ch1	ch2	ch3
0	0	0	0	0	0	0
0.01	84	21	137	2	1.6	1.6
0.02	168	42	276	2.1	2.2	1.7
0.03	252	63	385	2.4	2.4	2
0.04	336	84	500	2.5	3	2.6
0.05	420	105	618	3	3.6	3.6
0.06	504	126	698	3.8	3.8	3.7
0.07	588	147	775	3.9	4.2	4.5
0.08	672	168	850	4.4	4.1	4.8
0.09	756	189	893	4.6	4.3	5.1
0.1	840	210	960	4.6	4.7	5.6
0.2	1680	420	1120	6.3	6.3	7.8
0.3	2520	630	1170	9	7.8	7.9
0.4	3360	840	1180	10.3	8.2	7.7
0.5	4200	1050	1200	13.5	10.5	7.9
0.6	5040	1260	1210	19	16	9.7
0.7	5880	1470	1210	27	22.7	14.4
0.8	6720	1680	1220	35	30.2	20.5
0.9	7560	1890	1220	38.4	33.5	22.8
1	8400	2100	1230	41.5	35.1	23

S(mv/fc) (single ended)	5.94	0.018	0.015	0.010
		0.31%	0.26%	0.16%



Channel 3 to ch[0:2] crosstalk

	approx	2100	d3			
att factor	pe equiv	Qin(fc)	ch0	ch1	ch2	ch3
0	0	0	0	0	0	0
0.01	84	21	14	17	18	149
0.02	168	42	14	17	19	291
0.03	252	63	14	16	20	403
0.04	336	84	14	16	20	521
0.05	420	105	14	16	20	621
0.06	504	126	15	16	21	703
0.07	588	147	15	16	21	775
0.08	672	168	15	17	22	848
0.09	756	189	17	17	23	891
0.1	840	210	17	17	26	937
0.2	1680	420	23	24	39	1000
0.3	2520	630	30	31	52	1030
0.4	3360	840	35	35	68	1050
0.5	4200	1050	39	39	84	1060
0.6	5040	1260	42	42	98	1060
0.7	5880	1470	45	45	113	1070
0.8	6720	1680	46	48	141	1070
0.9	7560	1890	46	48	153	1070
1	8400	2100	51	51	173	1080

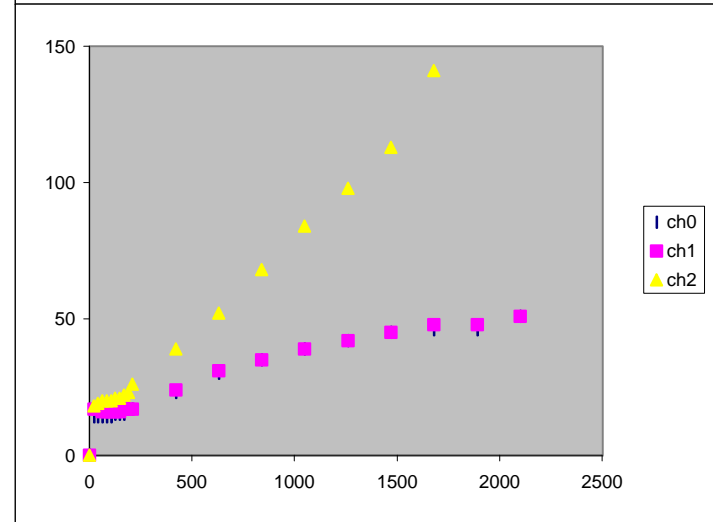
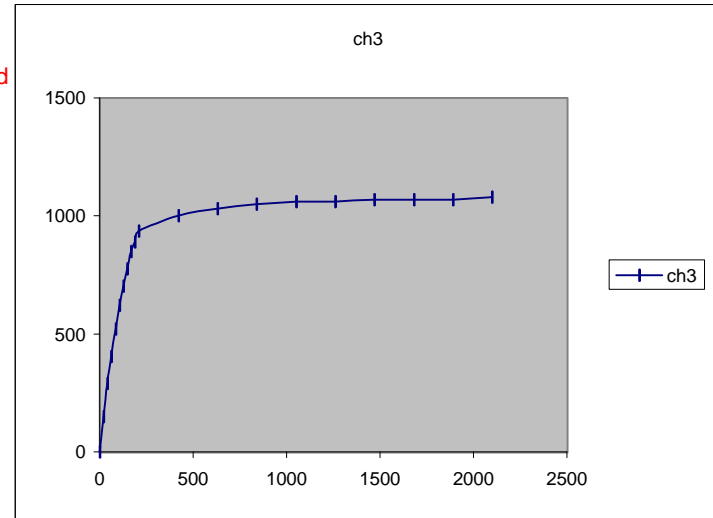
S(mv/fc) (single ended)	0.021	0.020	0.074	6.171
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Note: Entire chip is powered up. Charge injection into Channel 3

chip06

PRELIMINARY RESULTS!

Threshold



Channel 3 to ch[0:2] crosstalk

att factor	approx pe equiv	2100 Qin(fc)	d3			
			ch0	ch1	ch2	ch3
0	0	0	0	0	0	0
0.01	84	21			1	149
0.02	168	42			3	291
0.03	252	63			3	403
0.04	336	84			3	521
0.05	420	105			4	621
0.06	504	126			7	703
0.07	588	147			7	775
0.08	672	168			9	848
0.09	756	189			9	891
0.1	840	210	4	5	11	937
0.2	1680	420	11	11	27	1000
0.3	2520	630	14	17	40	1030
0.4	3360	840	20	20	52	1050
0.5	4200	1050	21	25	69	1060
0.6	5040	1260	25	26	81	1060
0.7	5880	1470	25	28	96	1070
0.8	6720	1680	30	32	121	1070
0.9	7560	1890	30	32	134	1070
1	8400	2100	33	34	158	1080

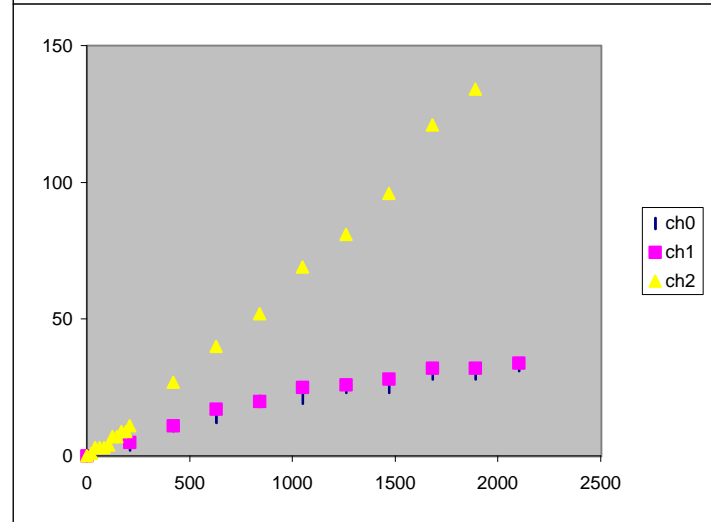
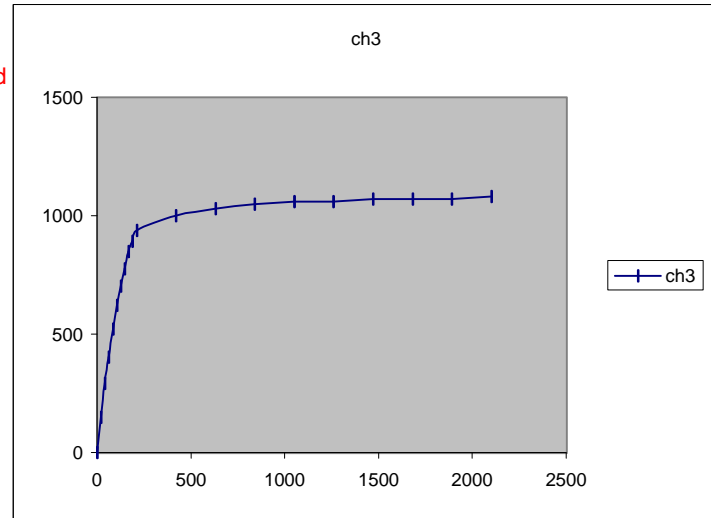
S(mv/fc) (single ended)	0.015	0.016	0.072	6.171
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DISC: Enabled
LVDS: Disabled

chip06

PRELIMINARY RESULTS!

Threshold



- Results & conclusions
 - (a) Good dc agreement with SPICE : operating point, offsets vs Monte Carlos
 - (b) Good pulse agreement with SPICE: peaking time, pulse shape, gain
 - (c) Xtalk improvement sufficient for ASD-lite, more work needed for final ASDs to understand left/right discrepancy
 - (d) Input protection (esd) needs some improvement for ASD-lite : Off-chip + on-chip protection needs to be $> 3\text{kv}$
 - (e) Packaging issues need investigating for ASD-lite ie chip on board vs. commercial IC package