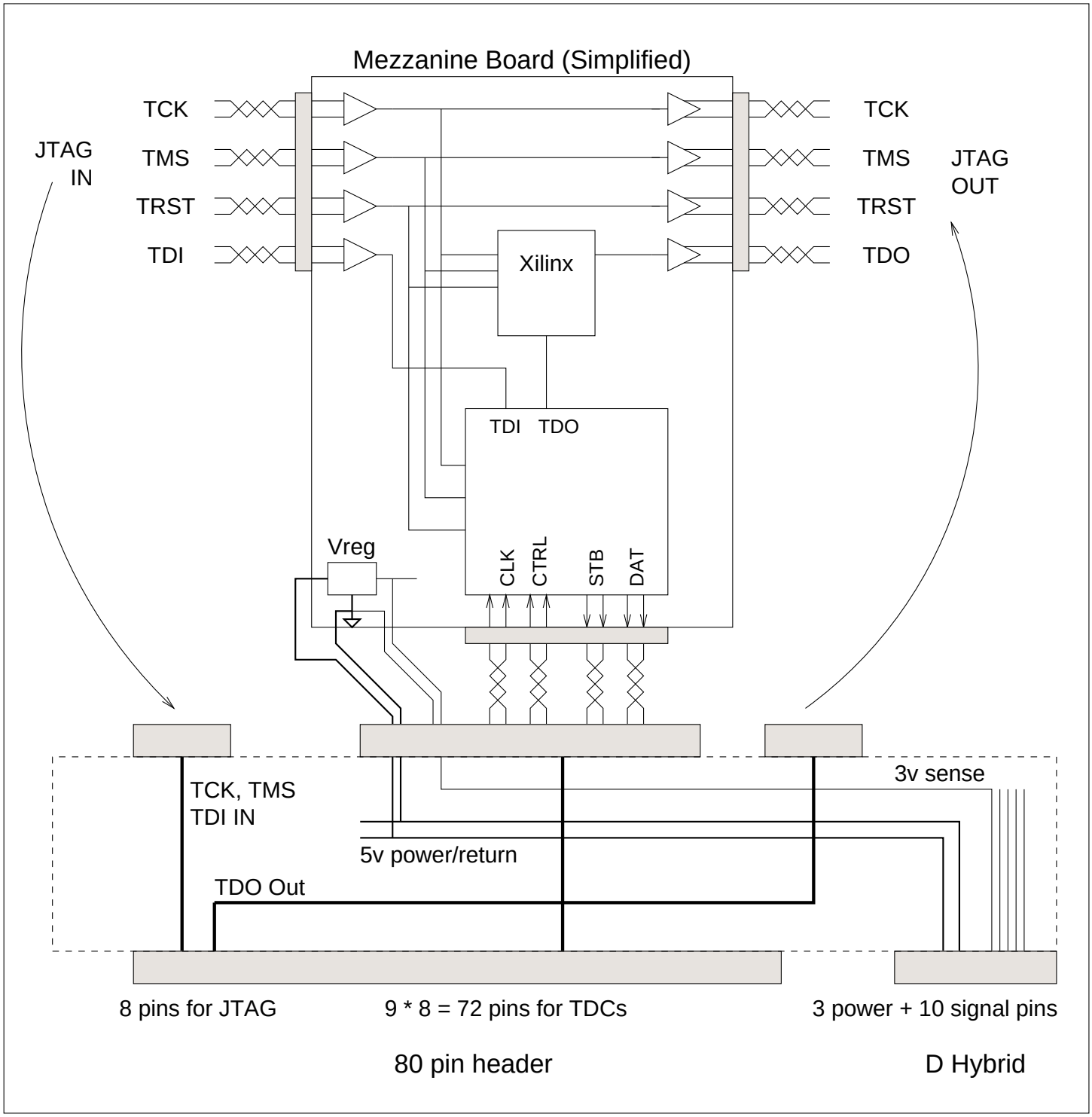
Mezzanine Board (Simplified)
JTAG IN
TCK
TMS
TRST
TDI
Xilinx
TCK
TMS
TRST
TDO
JTAG OUT
TDI TDO
Vreg
CLK
CTRL
STB
DAT
TCK, TMS
TDI IN
3v sense
5v power/return
TDO Out
8 pins for JTAG
9 * 8 = 72 pins for TDCs
3 power + 10 signal pins
80 pin header
D Hybrid