

ATLAS SLHC Upgrade

It is proposed to upgrade the LHC peak luminosity to $1.5 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$, 10 times nominal LHC luminosity. Ideally, the ATLAS detector would be upgraded to have the same performance at SLHC luminosity as at nominal. This requires many changes to the detector:

- Reduce background rates by changes to the beam pipe and improvements to shielding
- Improve radiation-tolerance of detectors and electronics, in many cases by replacing entire subsystems
- Increase bandwidth of front-end and readout electronics to minimize pile-up and handle 10x increase in event rate

Most work to date has focused on the central detector. However, much of the MDT (monitored drift tube) system would also need to be replaced for SLHC. Boston University played a key role in the development of the original system, and we expect to also participate in an upgraded system.

Summary of Existing System

On-Chamber Electronics

The MDT system is comprised of roughly 360,000 pressurized aluminum drift tubes 30mm in diameter. MDTs are arranged in super-layers of 3 or 4 tubes, with pairs of super-layers assembled to a support structure to form a “chamber”. There are a total of about 2000 such chambers. For nominal LHC conditions, the tubes must operate with a background rate of up to 300 kHz per tube (500 Hz/cm^2), and provide track resolution of $80 \mu\text{m}$ or better.

Each group of 24 MDTs is connected to a “hedgehog” circuit board. At one end, HV is distributed. At the other end, 24 signals are decoupled from HV and routed to a mezzanine board which contains all the active front-end electronics. Each mezzanine board contains three full-custom CMOS front-end chips (the MDT-ASD, a joint Boston University/Harvard design) and one full-custom TDC chip (the AMT-3, a joint CERN/KEK design). The hedgehog and mezzanine boards are enclosed in a complete aluminum Faraday cage to minimize susceptibility to external noise sources. The on-chamber electronics layout is shown schematically in Illustration 1.

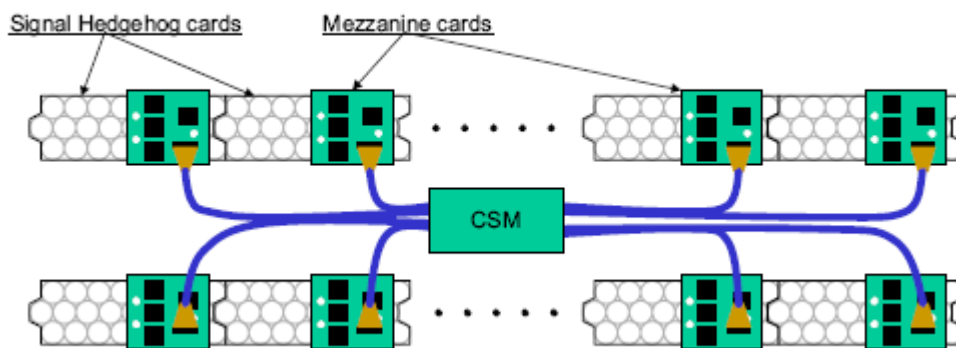


Illustration 1: On-Chamber MDT Electronics. Up to 18 Mezzanine cards are connected to a CSM on one chamber.

The MDT-ASD contains 8 signal processing channels, each providing a low-noise preamplifier (5000e rms coupled to 380 Ω terminated drift tube), a bipolar shaping amplifier, a leading-edge timing discriminator, a Wilkinson ADC (for time-walk correction) and LVDS outputs.

The AMT-3 provides 24 channels of time measurement with precision of 0.8ns, time-stamp recording, and trigger window matching.

Each chamber's readout is managed by a chamber service module (CSM, a University of Michigan design) which multiplexes the data from up to 18 mezzanine boards onto a 1.6 Gb/s optical fiber. The CSM also distributes clock, trigger and control information.

All of the on-chamber electronics was designed for radiation tolerance, and tested to radiation levels specified in ATLAS requirements documents. Individual requirements were specified for total ionizing dose, single-event upset sensitivity, and non-ionizing energy loss (neutron) sensitivity.

Off-Chamber Electronics

An MDT read out driver (MROD) VME module receives data streams from up to six MDT chambers. The MROD builds event fragments from the incoming sequences sent by the CSM, checks data integrity, and reports errors and inconsistencies. Event fragments are output via the read-out link (ROL), which is an optical link using the ATLAS-wide S-Link standard.

From this point on in the system, the DAQ is common to all ATLAS subsystems.

The off-chamber electronics is located in the USA15 shielded underground electronics area, and is thus not subject to any radiation-tolerance requirements.

Limitations of MDT System at SLHC

Most components of the MDT system fail or operate at drastically reduced efficiency at SLHC luminosity. The MDTs themselves suffer a serious loss of gain at high background rates due to space charge produced by positive ion accumulation [1], as shown in Illustration 2. In addition, the MDTs suffer a maximum dead-time set by the maximum drift time of about 800 ns. A faster gas and improvements in electronics could only improve this by (at most) 30-40%. For SLHC, an improvement of 10x is required.

- Gain Drop:

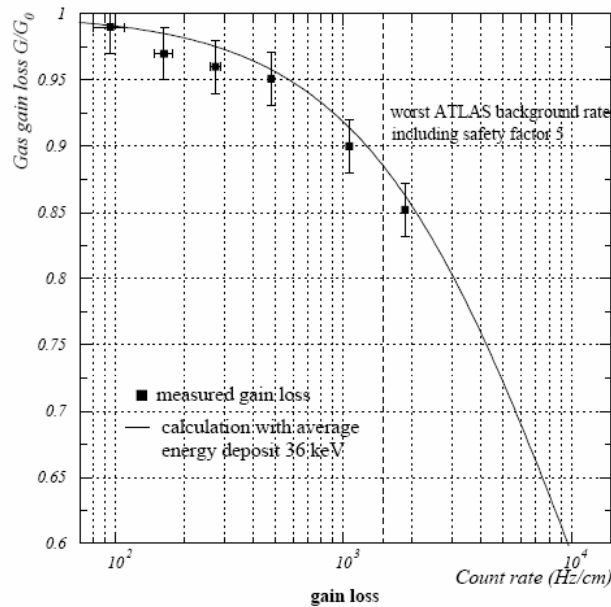


Figure 23: Gain drop versus background rate for a gas gain of $G_0 = 2 \cdot 10^4$. The solid line is calculated using the model introduced in section 6.2.1.

Illustration 2: MDT gas gain decrease due to space charge

The AMT-3 TDC output is limited to about 1MHz hit rate for 24 tubes. About 50% of this bandwidth is used at the design 100 kHz level 1 trigger rate in the highest-background regions for LHC. For SLHC, this bandwidth is exceeded by a factor of five. In addition, there are other limitations in buffering and logic which severely compromise the performance of the AMT-3 at SLHC rates. Some or all of these limitations could be addressed if the AMT-3 had been designed using programmable logic, but at the time this was not technologically feasible.

The CSM and ROD will also need significant upgrades. The data links between the mezzanine boards and the CSM, and the CSM and ROD must be replaced with higher bandwidth links.

The radiation tolerance of all on-chamber components must be re-evaluated for SLHC and many components will need replacement just for this reason.

Proposed Upgrade Tasks

We propose to collaborate with Harvard University (and perhaps University of Pennsylvania) to develop new on-chamber front-end electronics for an upgraded MDT system. We expect that many requirements for an upgraded system can be determined now and are independent of the details of the upgraded detectors themselves.

Upgraded MDT-ASD

Harvard would lead the effort to develop and new MDT-ASD. The basic signal processing chain would be quite similar to the existing design, but ported to a newer CMOS or BiCMOS fabrication process. Limitations and errors in the current design would be corrected. Boston University would play a consulting role in this task, assisting with simulation work and participating in the redesign of

portions of the original circuit designed at B.U.

Upgraded TDC

Boston University would develop a new TDC based roughly on the AMT-3 design, but implemented entirely in an FPGA (field-programmable gate array). We believe that all design requirements, including radiation tolerance, can be met with FPGA technology which can be reasonably foreseen on the timescale of SLHC. The current family of 90nm feature size FPGAs are inherently robust against permanent damage due to ionizing radiation. SEE (single-event effects) are the most serious problem, as they can corrupt stored data and even alter the logic configuration of the FPGA itself. There has been much work for space flight applications to develop triply-redundant logic techniques and “configuration scrubbing” to mitigate SEE. We propose to apply these techniques to the design of a fully-programmable TDC for ATLAS.

We can directly test SEE mitigation techniques at the Northeast Proton Therapy Center (in Boston) using a 160 MeV proton beam. We have successfully used this facility in the past to test many components of the existing MDT electronics for SEE.

References

[1] W. Riegler, “Rate Limitations of MDTs + Electronics”, Workshop on Upgrade of MDT electronics for SLHC, CERN, May 2007. *Indico* conference link:

<http://indico.cern.ch/conferenceDisplay.py?confId=16061>