Production Testing of ATLAS MDT Front-End Electronics

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Monitored Drift Tube (MDT) System

- Pressurized tubes: Ar/CO2 at 3 atm
- 3cm Aluminum tubes, 50μm Au-plated W-Re wire
- Length to 6m
- $Z_0 = 390 \, \Omega$
- Gas gain $\sim 2 \times 10^4$
- Maximum drift time $\sim 700$ ns
- Resolution spec (per tube) 80 μm
- Total of 360k tubes
MDT Chamber

Chamber isolated electrically from support and services. Only power/optical connections

- **LV Power**
  - 5V DC @ 60W
  - Isolated Ground (1k)

- **HV Power**
  - 3.5kV
  - Isolated Ground (1k)

- **Single Point Earth Ground**

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**TTC**
- Fanout

**Optical Fibers**

**ROD (DAQ)**

**Gigabit Optical Link (GOL)**

**Drift Tubes**

**Spacer Frame**

**Chamber Service Module**

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2003-10-02

E. Hazen - LECC 2003 - Amsterdam
MDT Electronics

Readout End Completely Shielded

- Drift Tubes
- Lower Faraday Cage
- Hedgehog PCB
- Upper Faraday Cage
- Mezzanine PCB
ASD Chip
1 of 8 channels

Transimpedance preamps

Signal

ZIN ≈ 120Ω

Dummy

Discriminator
(Bipolar shaper)

Wilkinson ADC

Control logic

LVDS

DACs
Calibration
Mode
Deadtime

Serial string register

Note: with grateful acknowledgement of work of Mitch Newcomer / U.Penn
AMT-3 TDC

- 24 Channels
- 0.78 ns least count
- Trigger matching logic
- LVDS serial I/O for control and data
- CMOS; rad-tolerant
Mezzanine Board

- Octal ASD
- Note 2D Barcode
- Discharge Protection
- Top/Bottom Layer
- PCB Ground Planes
- AMT-3
- TDC
- Power, I/O Connector
- Digital, Analog Voltage Regulators
Chamber Service Module

• Multiplex up to 18 x 24 channels via optical fiber
• JTAG control of front-ends
• TTC (trigger/clock) signals distribution
ASD Production

• Packaged ICs purchased
• 72k parts tested in 3 months on home-made automatic tester
• 3-5 sec per chip test time (no robotic loader)
• Tester cost about $100k including 1 m-yr University engineering (vs $500k for lower-performance commercial tester)
• Detailed test results kept in database
ASD Tester Overview

High-level commands \textit{i.e.}:
- Read preamp input levels
- Measure noise rate

High-level result data \textit{i.e.}:
- Measured DC levels
- Measured noise rate

Controller FPGA (XC2V1000):
- 16ns clock period
- 4ns TDC (DLL)
- Floating-point timer (20Hz-20MHz)

PC Parallel Interface

Input Fifo

Commands

Output Fifo

Data

LVDS (Outputs)

Test Socket (daughter board)

Serial i/o

DC

Analog support DACs, ADCs, Multiplexers

Command Processor:
- 16ns clock period
- 4ns TDC (DLL)
- Floating-point timer (20Hz-20MHz)
ASD Tests

• Serial I/O Test to verify JTAG interface
• DC (voltage/current) tests:
  – Preamp input voltage (self-bias point)
  – Bias Voltage Generator sweep
    • Can extract $K_P$ and $K_N$
  – LVDS Driver Output $V_{DIFF}$ and $V_{CM}$
  – Power Supply Current
• AC (dynamic) tests:
  – Wilkinson ADC parameters
  – Programmable deadtime vs setting
  – Threshold sweep
    • Vary discriminator threshold and measure noise hit rate
    • Fit results to Gaussian
    • Extract $V$(offset), Sigma and noise rate at threshold=0
• All results saved to database for long-term reference
Threshold Sweep Test
(Example of One Test)

Noise vs threshold sweep
- Gaussian fit gives
  - Sigma
  - Discriminator offset voltage
  - Peak hit rate
- Test takes ~2 sec
- 2 channels simultaneously $\rightarrow$ 4 seconds
- Grand total test time $\rightarrow$ < 5 seconds

This test is an effective “go/no-go” test of the entire analog chain.
Threshold Sweep Test Implementation

Loop over threshold
Settings from –40 to 40mV (software loop)

Measure time to record 32 hits using floating-point Timer (FPGA logic)

Effective range from 20Hz to 20MHz

Controlled by FSM
Implemented using StateCAD™
Threshold Sweep Test
Results: Offsets

- Channel-to-channel spread of DC offsets at discriminator is most useful output of this test
- Primary parameter for “quality” grouping of ASDs

Cut at 12mV
Gives 75% yield
ASD Test Result Summary

Test Results for 72k ASDs

- 75% Good
- 18% Out of Tolerance
- 6% Partially Functional
- 1% Dead

- Overall 93% yield of functional parts
- Most “Out of Tolerance” rejects due to threshold offsets > 12mV
Board Production Plan

• Assemble in Israel, ship to Boston
• Test flow:
  – Serialize with 2D Barcodes
  – Burn-in (24hr at elevated temp)
  – Full Functional Test
  – Pack and Ship
Mezz Board Test Setup

Sites for 15 Boards

Readout Adapter

VME Readout PC, Software...

Test Pulse Injector
Mezz Board Testing

- Full test of 15 boards in a few minutes
- JTAG programming test
- Threshold sweep similar to chip test
  - Termination resistor seen; confirms board connectivity
  - Verifies TDC and DAQ logic functionality
- Bonus:
  - Individual boards can be identified with 99.999% accuracy by threshold offset “signature”
Board Burn-In Facility

- 24-hour elevated temp burn-in
- Continuous monitoring of current, voltage, temp.
  Summary data stored indefinitely in database

Enclosed Cabinet Rack

10 Subracks
(3U std)

Power Supply

PC with I/O Card
(Digital/Analog)
Board Burn-In Data

- “Strip Chart” record:
  - Temperature (each board)
  - Analog, Digital regulator output
  - Analog, Digital supply current
- Problems such as tantalum cap failures show clearly
- Max/Min/Mean/Sigma of each quantity stored in permanent database
Database

- Extensive set of measured parameters kept for each channel/chip/board
- Web access with query/plot facilities
- Tied to barcode ID of each chip and board
- Some sample plots:

Scatterplot of FET $K_N$ vs $K_P$

Histogram of Threshold Offsets
Summary

• Custom test hardware for production of 360k channels built
• 72k chips tested in 3 months
• Test/burn-in capacity of 150 boards/day
• On track to start delivery later this year
• Would we do it this way again? Yes!